



Revising last lecture

- In high-speed designs, conductors cannot be considered as simple interconnections.
- For a normal FR4 PCB material with a dielectric constant velocity of electromagnetic waves is 1.41 m/s. Indicate the order of magnitude of PCB traces that can be considered simple connections when transporting 1GHz signals.

$$t_r \approx 0.1 \times \frac{1}{1 \times 10^9} = 0.1 \text{ ns}$$

$$1.41 \times 10^8 \times 0.1 \times 10^{-9} = 1.41 \text{ cm}$$



Signal Integrity



Outline

- Signal integrity
- Signal integrity for high speed design
- Fundamental concepts to understand signal integrity in high speed design: frequency/time, inductance, capacitance, mutual inductance, mutual capacitance, crosstalk, ground bounce, etc



Signal Integrity

- The signal integrity issue is in general and currently associated with high speed **frequency** (high speed signals). However, the signal integrity issue is not necessarily related to frequencies.
- A signal integrity problem exists whenever the signal begins to lose its quality.
- Two of the more obvious and common ways a signal can lose integrity are:
 1. when it becomes **distorted**. Signal distortion typically means that the waveform of interest begins to change shape.
 2. when the **signal-to-noise ratio** (S/N) begins to **degrade**. S/N issues come into play whenever an unwanted noise becomes detectable and/or interferes with the signal we are concerned with.
This second item is not directly related to frequency.

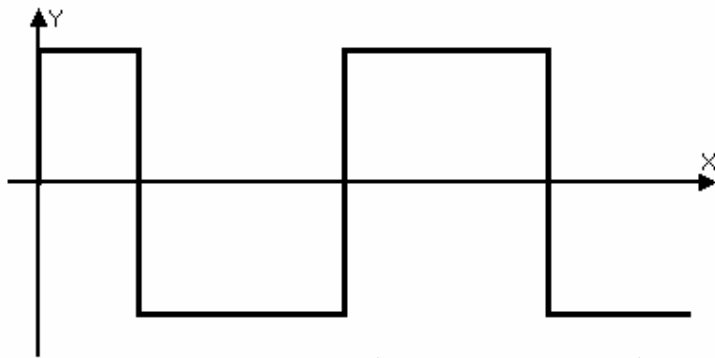


Signal Integrity

- **Distortion** typically means that the waveform of interest begins to change shape. Different Fourier components are diminished by different amounts.
 - Analog signals can be very sensitive to distortion. A change in the waveform will often be seen or heard. Audio systems specify harmonic distortion, which relates to the “purity” of the audio signal as it is processed
- **S/N issues** come into play whenever an unwanted noise becomes detectable and/or interferes with the signal we are concerned with.
 - Analog signals can be very sensitive to noise interference. For example, hearing the 50 Hz (electrical network) in the audio system is a signal integrity problem.

Signal integrity for high speed design

- Distortion

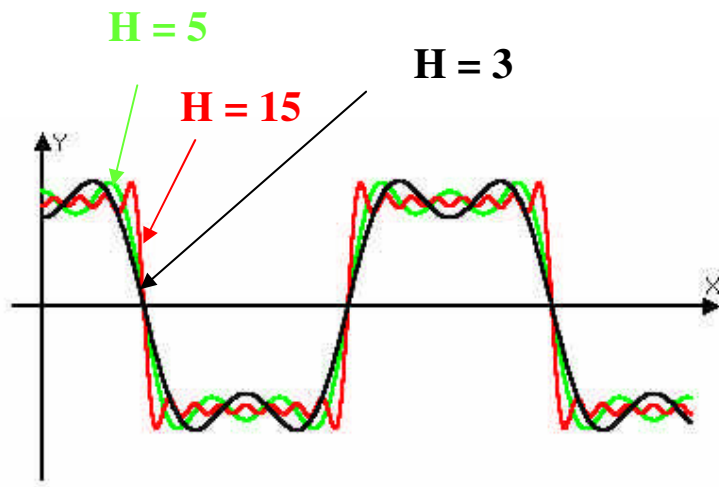


$$Y(t) = \cos(\omega t) - \frac{1}{3}\cos(3\omega t) + \frac{1}{5}\cos(5\omega t) - \frac{1}{7}\cos(7\omega t) + \dots$$

- In a real system square waves are not perfect. They are really characterized by a rise (fall) time.

Signal integrity for high speed design

- To reproduce signals with small rise (fall) time, high bandwidth is required for the system.



$$Y(t) = \cos(\omega t) - \frac{1}{3} \cos(3\omega t)$$

$$Y(t) = \cos(\omega t) - \frac{1}{3} \cos(3\omega t) + \frac{1}{5} \cos(5\omega t)$$

$$Y(t) = \cos(\omega t) - \frac{1}{3} \cos(3\omega t) + \frac{1}{5} \cos(5\omega t) - \frac{1}{7} \cos(7\omega t) + \frac{1}{9} \cos(9\omega t) - \frac{1}{11} \cos(11\omega t) + \frac{1}{13} \cos(13\omega t) - \frac{1}{15} \cos(15\omega t)$$



Signal integrity for high speed design

- Signal to noise issues
 - Conductors have inductance. The voltage generated across an inductor can be approximated

$$V = L \frac{di}{dt} = L \frac{di}{t_r}$$

- V gets larger as t_r gets smaller. V can be considered a noise voltage.
 - Similar analysis can be done for stray capacitance.
- Therefore, signal integrity gets worse as rise (fall) time gets smaller



Signal integrity for high speed design

- Signal integrity is not necessarily related to frequencies, but signal integrity becomes a problem:
 - when the system bandwidth limits rise (fall) times: distortion
 - when the rise time decreases to the point where the parasitic inductances and capacitances begin to result in noise signals that become troublesome: S/N issues



Exercise

- How to compute the total harmonic distortion of a periodic signal?

Periodic signal $v(t)$ with frequency ω

$$v(t) = V_1 \sin \omega t + V_2 \sin 2\omega t + V_3 \sin 3\omega t + +V_4 \sin 4\omega t + \dots$$

$$THD = \sqrt{\frac{V_2^2}{V_1^2} + \frac{V_3^2}{V_1^2} + \frac{V_4^2}{V_1^2} + \dots}$$

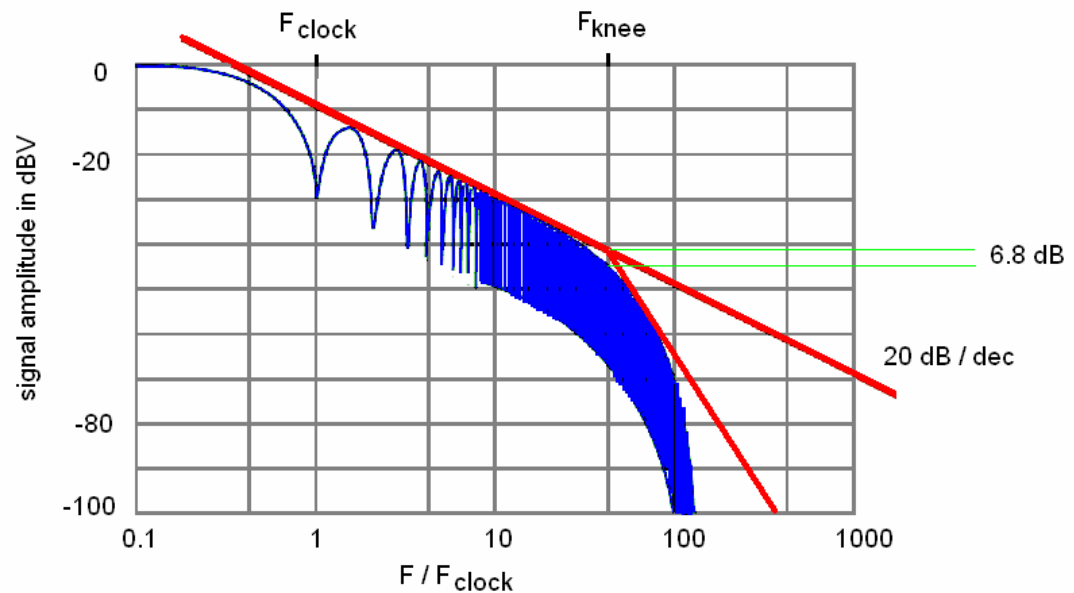


Frequency/Time

- At low frequencies a wire (a PCB trace) short two circuits.
- At high frequencies the same wire can be an inductor.
- From very low frequencies to high frequencies (very short intervals of time) electrical parameters change can occur. Example of a wire:
 - at 1 kHz $R = 0.01 \, \Omega$, $X_L = 0 \, \Omega$
 - at 1 GHz $R = 1 \, \Omega$, $X_L = 50 \, \Omega$
- Few electrical parameters remain constant across 10/ 20 decades
- Big changes in performance occur in electric circuits when pushed to the upper end of their operating frequency range.
- How high range of frequency matters?

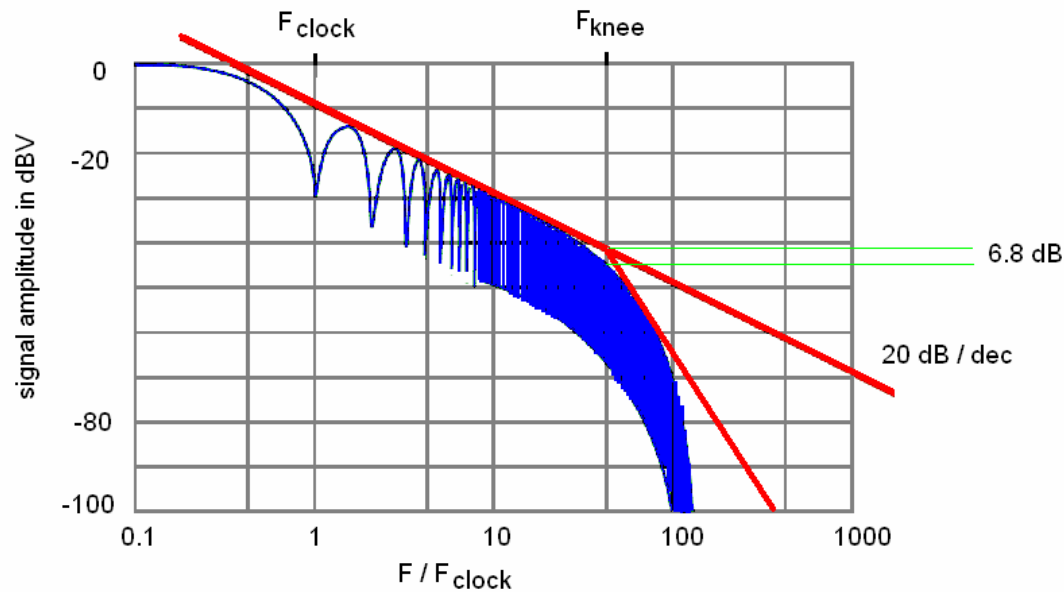
Frequency/Time

Power spectral density (PSD) of a random digital pulse train
with $t_r = 0.01 \times T_{CLK}$



- Nulls at multiples of f_{CLK}

Frequency/Time



$$F_{\text{knee}} = \frac{0.5}{T_r}$$

- The amplitude (in dB) decreases at a rate of 20 dB per decade for $F < F_{\text{knee}}$
- At F_{knee} the amplitude is 6.8 dB below the 20 dB/decade line
- Above F_{knee} the amplitude falls away rapidly.



Frequency/Time

- F_{knee} can be estimated as

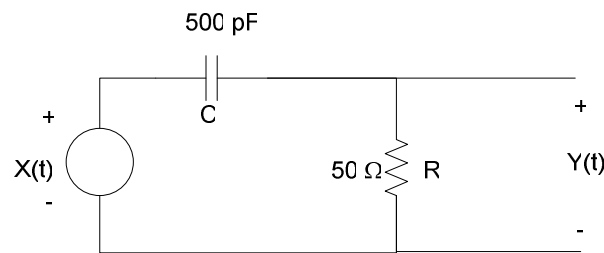
$$F_{\text{knee}} = \frac{0.5}{T_r} \quad T_r \text{ pulse rise time (10\%-90\%) (or fall time)}$$

- F_{max} (3 dB frequency) also used as F_{knee}

$$F_{\text{max}} = \frac{0.35}{T_r} \quad \text{less conservative: RL, RC first order circuits}$$

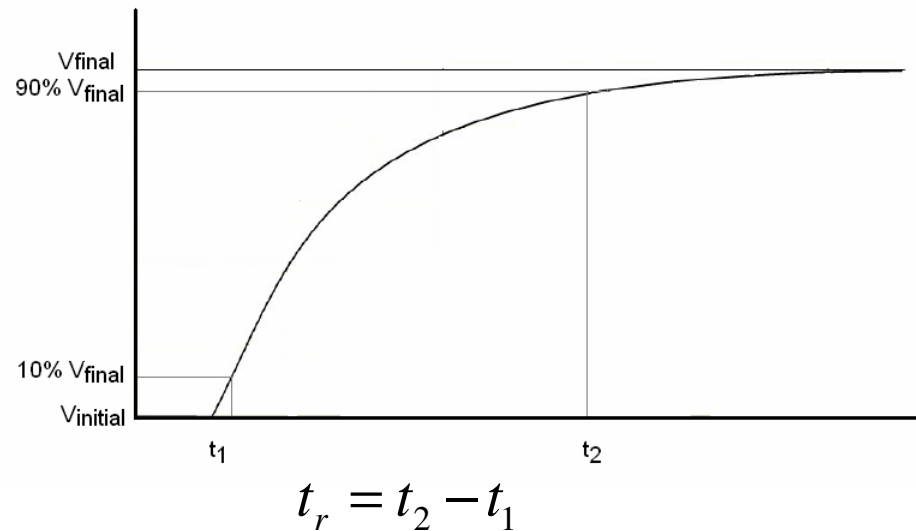
Exercise

How can we obtain $F_{\max}$ (3 dB) in a first order circuit?



$$F_{3dB} = \frac{1}{2\pi RC} = \frac{1}{2\pi \tau}$$

Exercise



$$\begin{cases} 0.1V_{final} = V_{final} - (V_{final} - V_{initial})e^{-\frac{t_1}{\tau}} \\ 0.9V_{final} = V_{final} - (V_{final} - V_{initial})e^{-\frac{t_2}{\tau}} \end{cases}$$

$$\tau = \frac{t_r}{\ln 9}$$

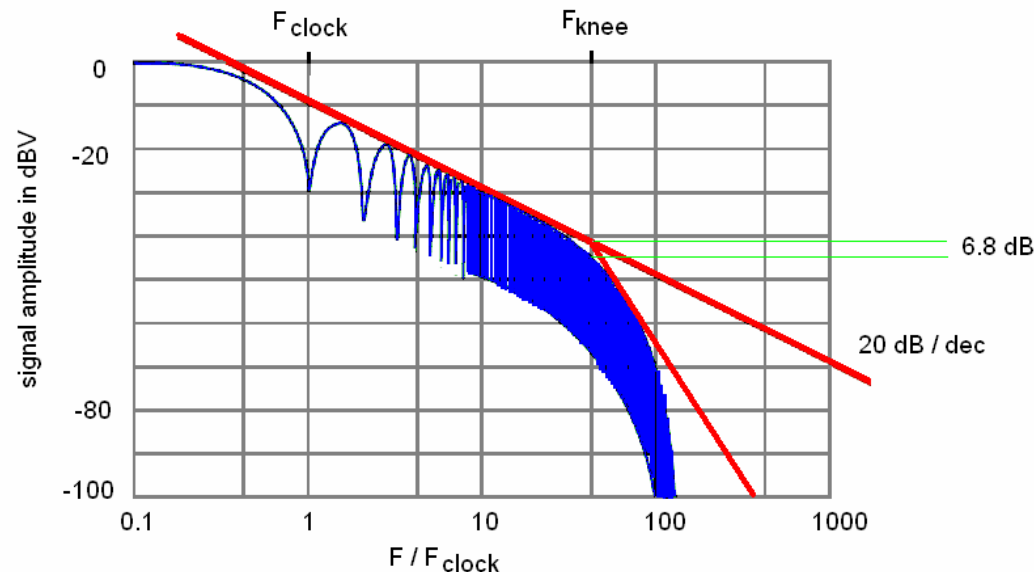
$$F_{3dB} = \frac{1}{2\pi\tau} = \frac{\ln 9}{2\pi} \frac{1}{t_r} \approx \frac{0.35}{t_r}$$



Frequency/Time

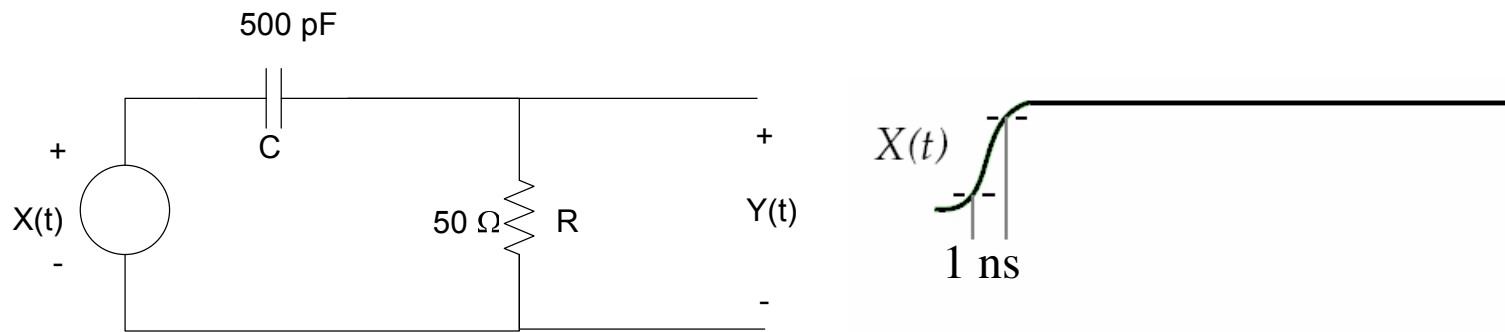
- F_{knee} is an imprecise measure that can be used to understand the performance of a high speed digital signal.
- F_{knee} helps to classify frequency-sensitive aspects in design as:
 - totally insignificant
 - merely worrisome
 - completely devastating.
- F_{knee} is the defined as the frequency bellow which most energy in digital pulses concentrates.

Frequency/Time



- The important time domain characteristics of any digital signal are determined primarily by the signal's spectrum below F_{knee} :
 - Any circuit which has a flat response up to and including F_{knee} will pass a digital signal practically undistorted.
 - The behavior above F_{knee} of a digital circuit will have little effect on how it processes digital signals.

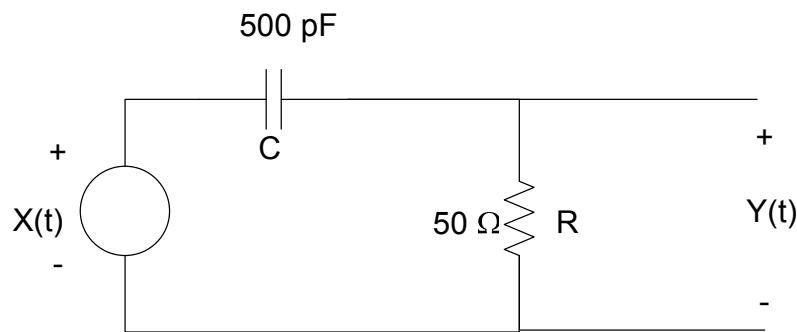
Frequency/Time



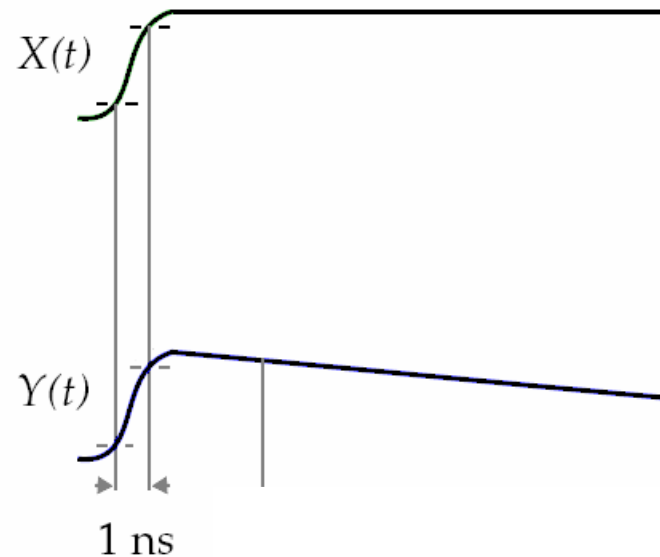
Will the signal $X(t)$ be distorted?

Frequency/Time

- Frequency analysis



$$f_{3dB} = \frac{1}{2\pi RC} = 6.37 \text{ MHz}$$

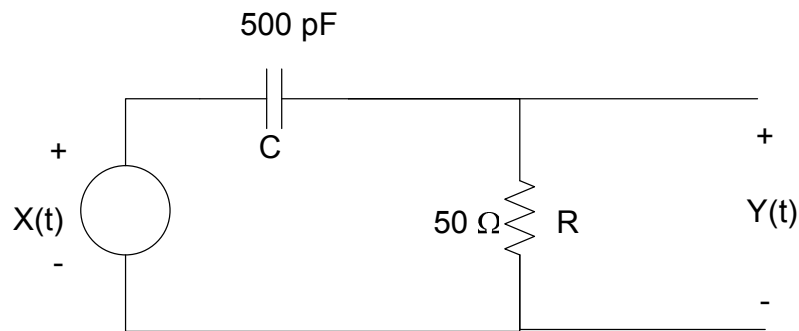


$$F_{knee} = \frac{0.5}{T_r} = 5 \times 10^8 = 500 \text{ MHz}$$

- The behavior of a circuit at knee frequency determines its processing of step edge

Frequency/Time

- Time analysis

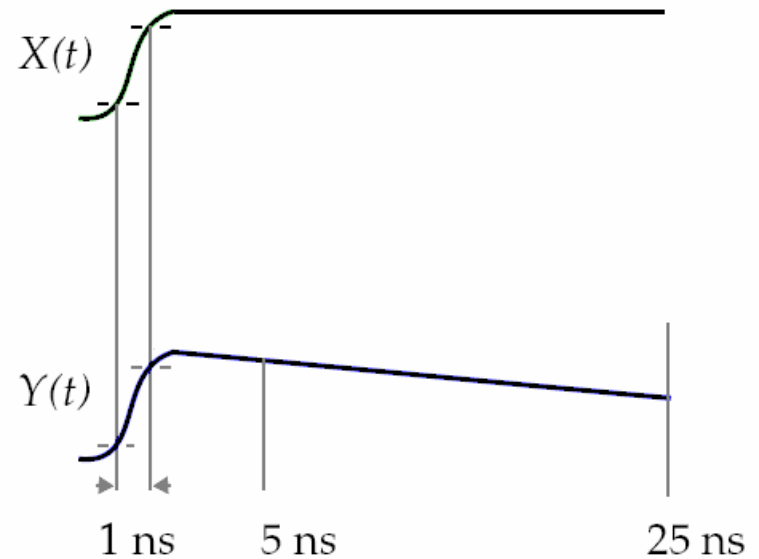


$$X_c = \frac{1}{2\pi f_{knee} C} = \frac{T_r}{2\pi 0.5 C} = \frac{T_r}{\pi C}$$

$t = 1 \text{ ns}$, reactance is 0.6Ω

$t = 5 \text{ ns}$, reactance is 3Ω

$t = 25 \text{ ns}$, reactance is 15Ω .





Frequency/Time

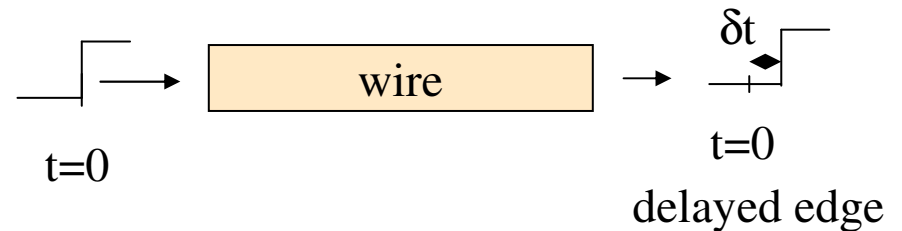
Summarizing:

- The response of a circuit at high frequencies affects its processing of short time events.
- The response of a circuit at low frequencies affects its processing of long term events.
- Most energy in digital pulses concentrates below the F_{knee} frequency
- The behavior of a circuit at F_{knee} determines its processing of a step edge
- The behavior of a circuit above F_{knee} hardly affects digital performance

Time/distance

- Electrical signals propagate in wires at a speed that depends on the surrounding medium:

- propagation delay (ps/in)
- propagation velocity (in/ps)



- What is the propagation delay and propagation velocity of air waves?

85 ps/ in

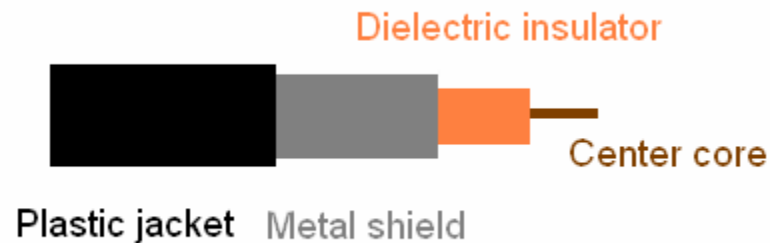
11.8 in/ns (3×10^8 m/s)

- Propagation delay is proportional to the square root of the relative dielectric constant of the surrounding medium

$$\text{Propagation delay} = 85 \sqrt{\epsilon_r} \text{ ps/in}$$

Time/distance

- Cables use foam and ribbed material to reduce the dielectric constant



Dielectric Type	Time Delay (ps/in)	Propagation Velocity (% of c)
Solid Polyethylene (PE)	129	65.9
Foam Polyethylene (FE)	106	80
Foam Polystyrene (FS)	93	91
Air Space Polyethylene (ASP)	101-122	84-88
Solid Teflon (ST)	122	69.4



Lecture exercise

- What is the propagation velocity in a trace in FR4 PCB? Consider That FR4 has a relative dielectric constant of 4.

$$\text{Propagation velocity} = 11.8 / 2 \text{ in/ns} \approx 6 \text{ in/ns}$$

Time/distance

- Propagation delay on PCB depend on surrounding dielectric constant

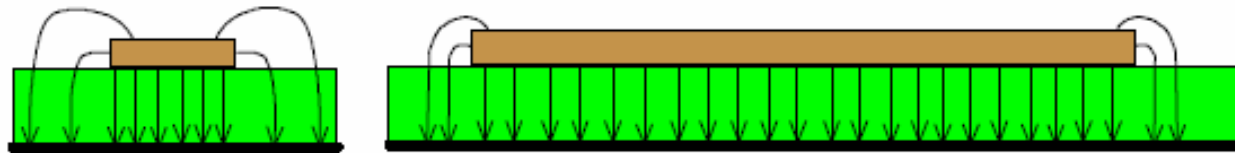
Medium	Propagation delay (ps/in)	Dielectric constant
FR4 (outer trace)	140-180	2.8-4.5
FR4 (inner trace)	180	4.5
Alumina PCB, inner trace	240-270	8-10

- Outer traces share their electric between the air on one side and the substrate material on the other side. The dielectric constant will be halfway between 1 and 4.5.
- Propagation delay on PCB depend also on traces geometry .

Time/distance

- Traces geometry determines whether the electric field stays in the board or goes into the air.

Ex: microstrip



- For the wide trace, most of the field lines will be in the dielectric between the trace and the plane. Only a small percentage of them above the trace are in the air. Since the propagation speed is slower in the dielectric, it is expected that the speed of the larger trace will be slower.



Time/distance

- Summarizing:
 - Propagation delay is proportional to the square root of the dielectric constant
 - The propagation delay of signal traveling in the air is 85 ps/in
 - Outer layer traces propagate faster than inner traces.



Lumped versus distributed systems

- The response of any system of conductors to an incoming signal depends greatly on whether the system is smaller than the effective length of the fastest electrical feature in the signal or vice versa.
- The effective length of a rising edge, depends on the time duration of the edge and its propagation delay:

$$l = \frac{T_r}{D} = \frac{1n}{180p} = 5.6 \text{ in}$$

l = length of rising edge in inches.

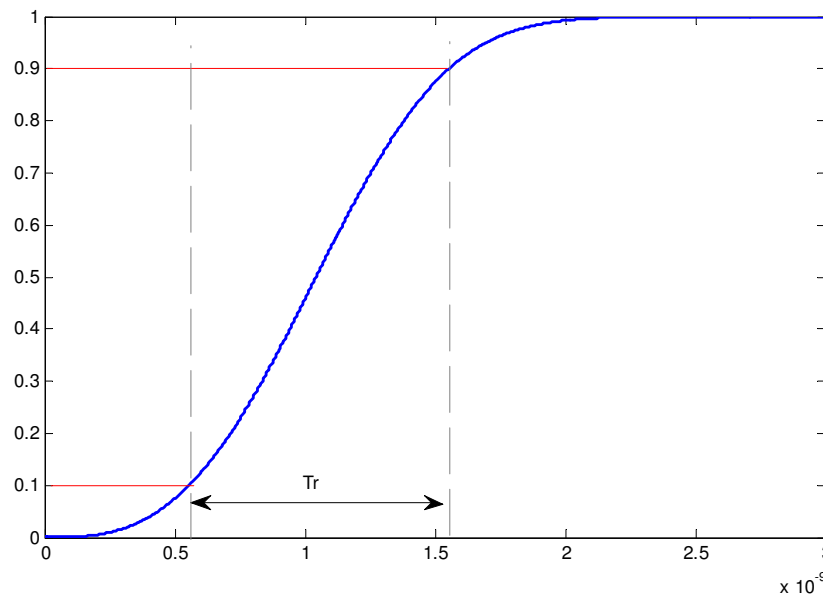
T_r = rise time in ps.

D = propagation delay in ps/inch (FR4
180ps/in.

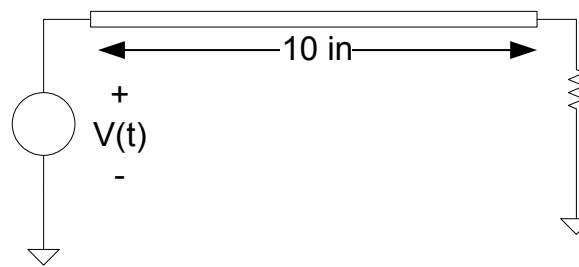
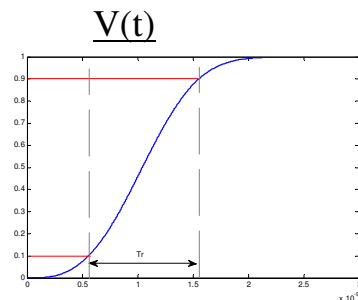
Lumped versus distributed systems

- Rising edge:

$$l = \frac{T_r}{D} = \frac{1n}{180p} = 5.6 \text{ in}$$

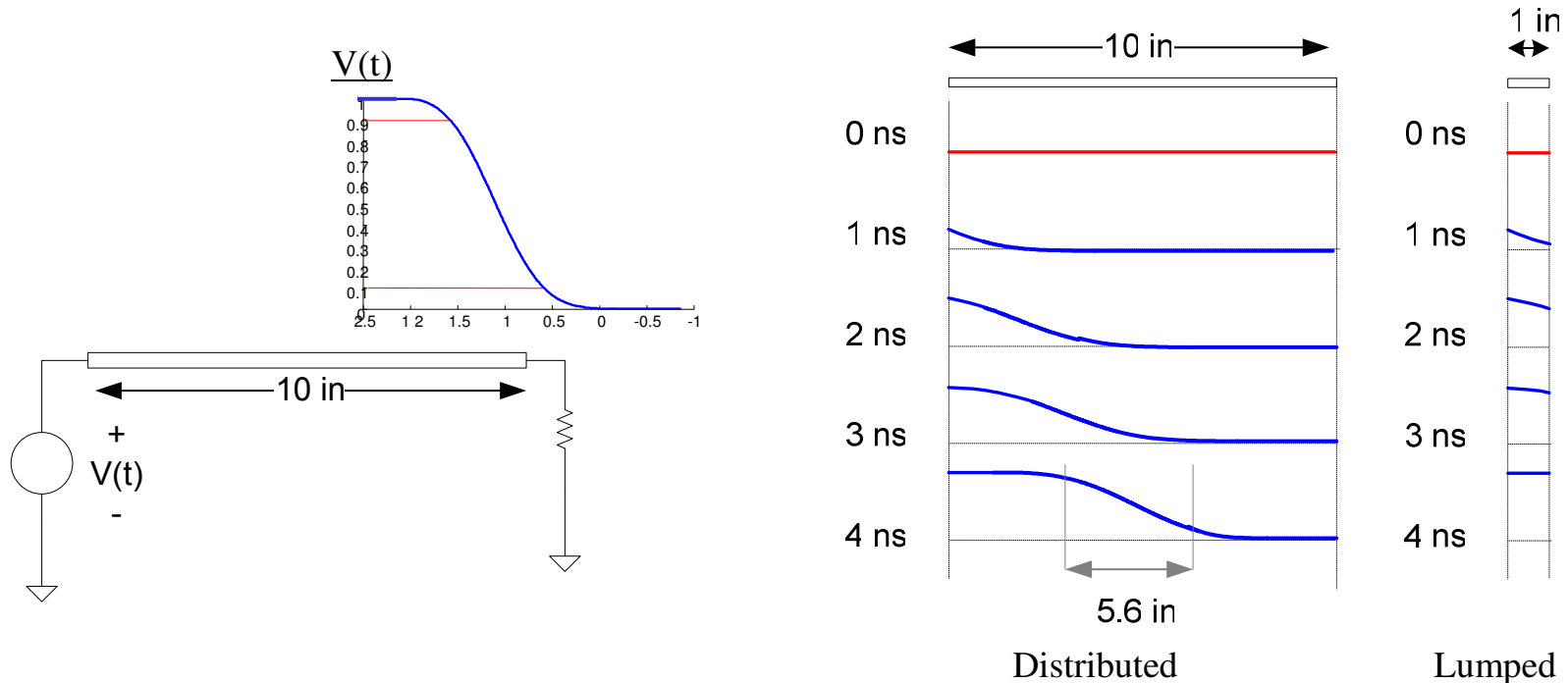


Lumped versus distributed systems



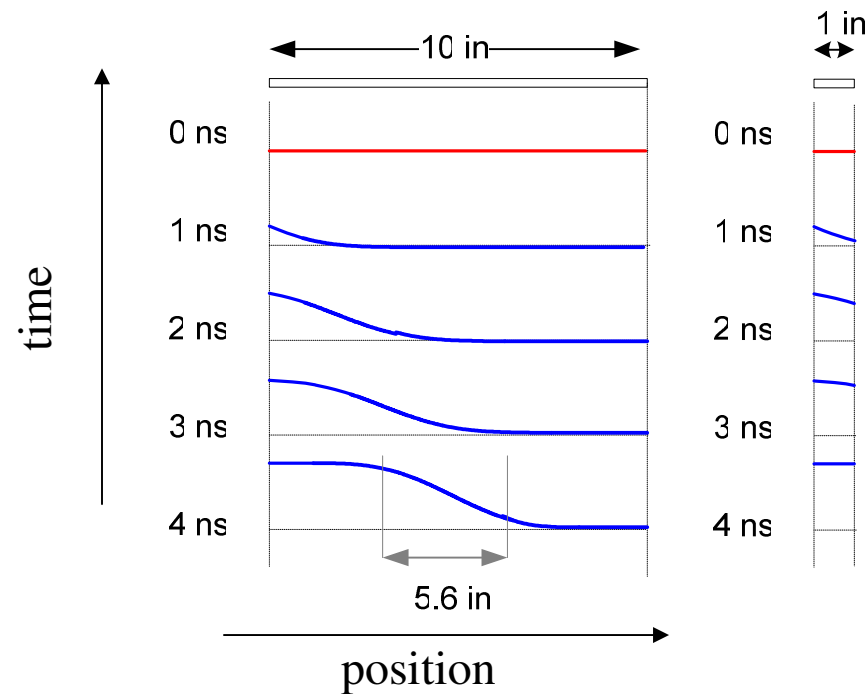
- Distributed systems: The pulse propagates along the trace, the potential is not uniform at all points.
- Classification (lumped or distributed) based in the ratio of the system size to rise-time size.

Lumped versus distributed systems



- Distributed systems: The pulse propagates along the trace, the potential is not uniform at all points.
- Classification (lumped or distributed) based in the ratio of the system size to rise-time size.

Lumped versus distributed systems



- In a distributed circuit voltages and currents are functions of position as well as time.
- Rule of thumb: if wiring is shorter than one-sixth of length of rising edge, the circuit behaves in a lumped fashion.



Lumped versus distributed systems

- Summarizing:
 - Length of rising edge

$$l = \frac{T_r}{D}$$

T_r = rise time in ps.

D = propagation delay in ps/inch.

- Wires less than $\frac{l}{6} \Rightarrow$ lumped circuit



Revising last lecture

- Why a wire in a cable or a trace on a PCB can not be considered a short-circuit for high frequencies?
- What are the more obvious and common ways to make a signal lose its integrity?
- The knee frequency of a signal is at 250MHz, what information does it give to a digital system designer?
- What is F_{knee} ? Is F_{knee} a precise measure?
- Does the knee frequency give any information about the long-term response of the circuit?
- What is the difference between:

$$F_{knee} = \frac{0.5}{T_r} \quad F_{max} = \frac{0.35}{T_r} ?$$



Revising last lecture

- Propagation of electrical signals depend on?
 - the medium (Propagation delay = $85 \sqrt{\epsilon_r}$ ps/in)
 - geometry of wires
- Air waves propagation delay and propagation velocity?

$$\frac{3 \times 10^{10} / 2.54}{3 \times 10^{12}} \text{ in / ps} = 11.8 \times 10^{-3} \text{ in / ps} \quad \frac{1}{3 \times 10^8} \text{ s / m} = \frac{10^{12}}{3 \times 10^{10} / 2.54} \text{ ps / in} = 85 \text{ ps / in}$$

- Compare propagation delay in outer and inner traces
- The length of a rising edge depend on? $l = \frac{T_r}{D}$
- Circuits with dimensions less than $l/6$ are considered lumped circuits or distributed circuits?



Lecture exercise

- A signal with a rising edge of 3ns is passed on a FR4-PCB inner trace. The maximum size of traces in this PCB is 5 in. Can we analyze the circuit as a lumped circuit?

$$l = \frac{3n}{180ps/in} = 16.7 in$$

$$\frac{l}{6} = \frac{16.7}{6} = 2.78 in$$

$$5 in > \frac{l}{6} = 2.78 in$$

The circuit **cannot** be analyzed as a lumped circuit (long traces).



Lecture exercise

- If the rise time is 6 ns, a 5 inch trace can be analyzed as a lumped circuit?

$$l = \frac{6n}{180ps/in} = 33.3 in$$

$$5 < \frac{l}{6} = 5.56$$

$$\frac{l}{6} = \frac{33.3}{6} = 5.56 in$$

The circuit **can** be analyzed as a lumped circuit (small traces).



Lecture exercise

A PCB trace has flat frequency response up to 100MHz.

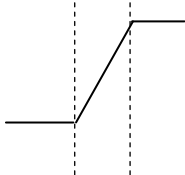
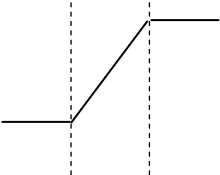
1. Find the shortest T_r of the signal that passes this trace without distortion.
2. Sketch the output of the PCB trace for a input clock edge with
 - a) rise time T_r ;
 - b) rise time much longer than T_r ;
 - c) rise time much shorter than T_r

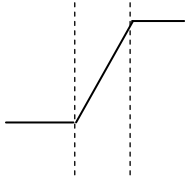
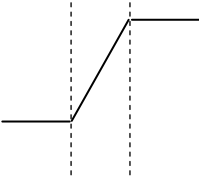
$$F_{knee} = \frac{0.5}{T_r} < 100MHz$$

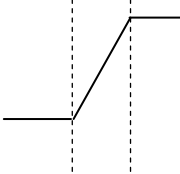
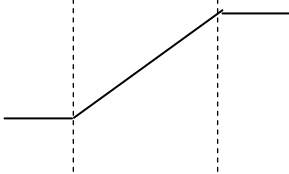
$$T_r > \frac{0.5}{100M} = 5ns$$

Lecture exercise

$$T_{output}^2 = \sqrt{T_{signal}^2 + T_{PCB}^2}$$

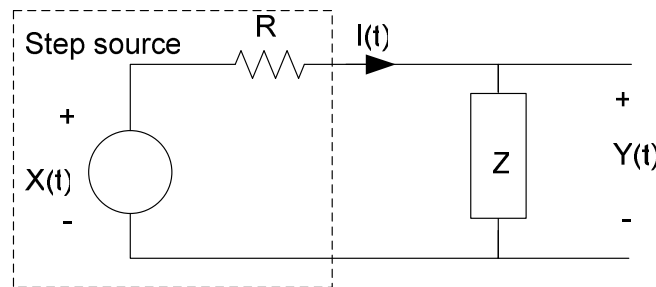


 $T_{signal} = T_{PCB} = T_r$
 $\sqrt{T_r^2 + T_r^2}$



 $T_{signal} \gg T_{PCB} = T_r$
 T_{signal}



 $T_{signal} \ll T_{PCB} = T_r$
 T_r

Reactance

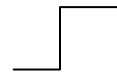
- Four concepts separate the study of high frequency to low speed digital circuits:
 - Ordinary capacitance (individual components):
 - Ordinary inductance (individual components)
 - Mutual capacitance (between two wires closed to each other)
 - Mutual inductance (between two curly wires)
- Time analysis: in digital signals, reactance is analyzed using the step response $Y(t)$.



Reactance

- Time analysis: it is possible to see what happens when a pulse hits a circuit:

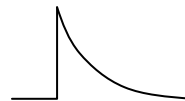
- Resistors have flat response.



- Capacitors have a response that starts at zero and rises to a full-valued output



- Inductors have a step response that starts at full value and decays back to zero





Reactance

- With the step response, it is possible to emphasize the characteristics of a circuit element in a particular frequency range.

- If the step rise time is T_r , the step response near $t = 0$ is related to the impedance magnitude near frequency F

$$F = \frac{0.5}{T_r}$$

- Averaging the step response over a time interval, we can estimate the impedance magnitude at lower frequencies.
- The final value of the step response indicates the impedance magnitude at DC.

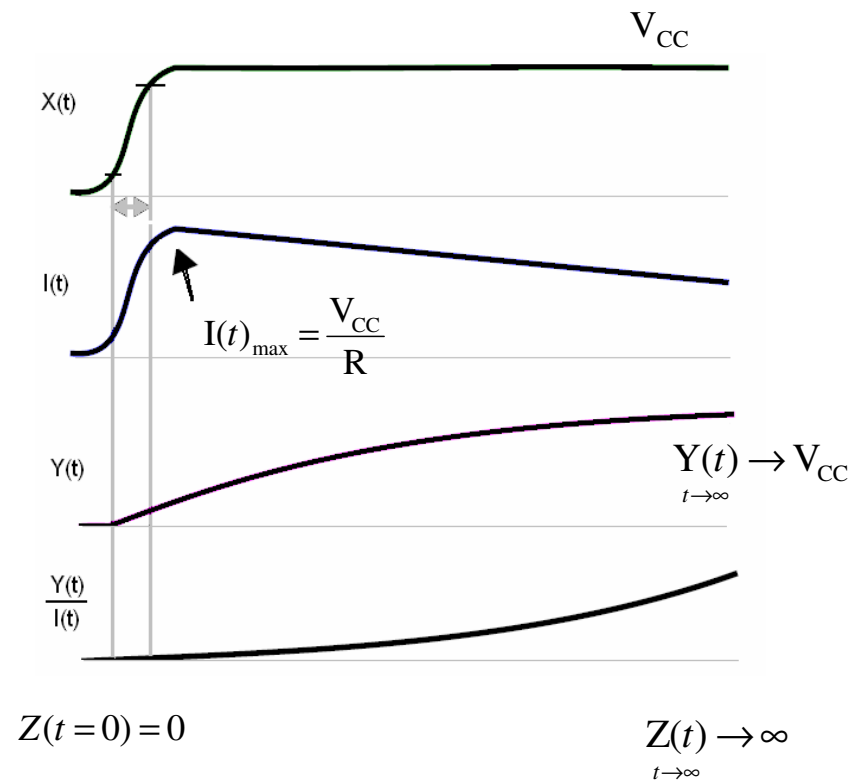
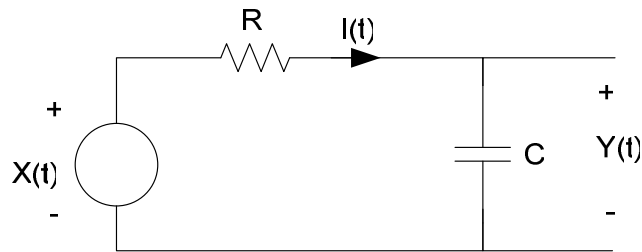


Reactance

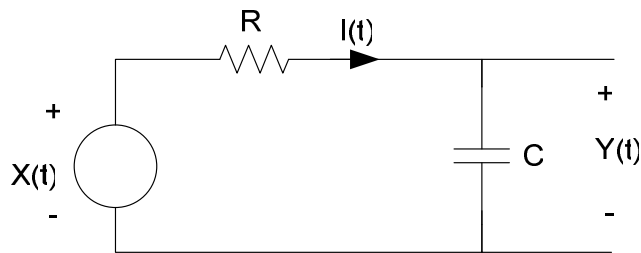
- The step response of some circuits elements display a capacitive effects when viewed at one time scale and inductive characteristics at a different time scale
- Adequately adjusting the rise time and the base step time, the step response can emphasize the behavior of a circuit in a particular frequency range.
- Example: the mounting leads on capacitors have enough inductance to look inductive at high frequencies. In the step response, a tiny pulse can be seen at time zero. After, the response is a normal capacitive ramp. However, if the rise time is set too slow, the small spike can not be seen. If the scope base time is too slow, it is also easy to miss the spike that is too short.

Ordinary capacitance

- Step response of a perfect capacitor



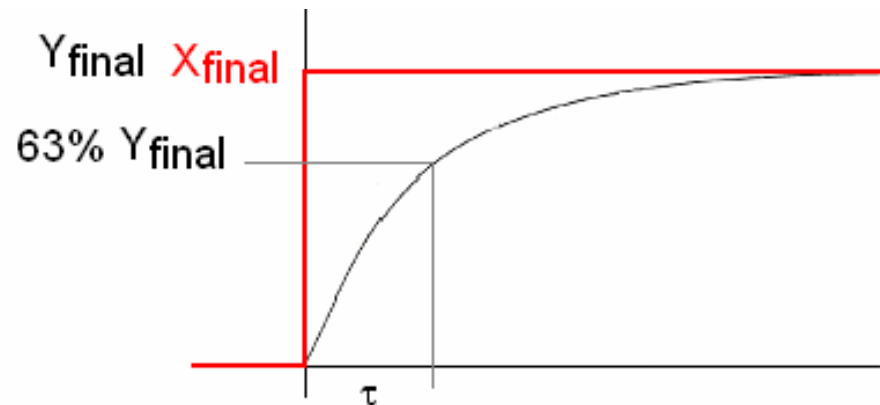
Ordinary capacitance



$$Y(t) = Y_{final} - Y_{final} e^{-\frac{t}{\tau}}$$

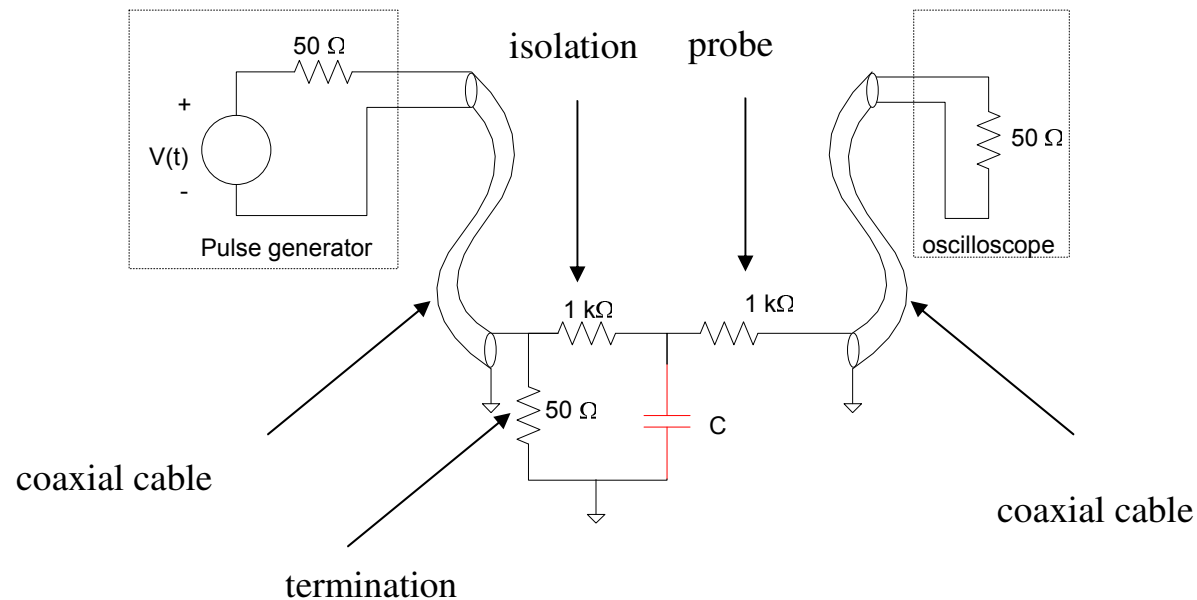
$$Y(\tau) = Y_{final} - \frac{Y_{final}}{e} \approx 0.63 Y_{final}$$

$$C = \frac{\tau}{R}$$

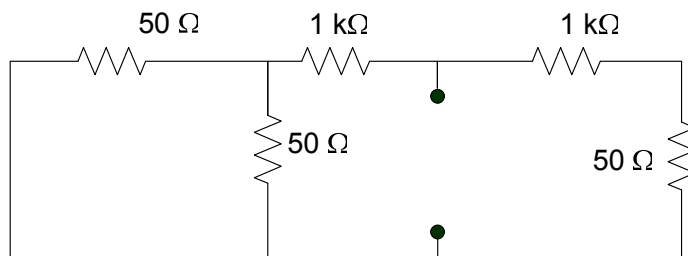
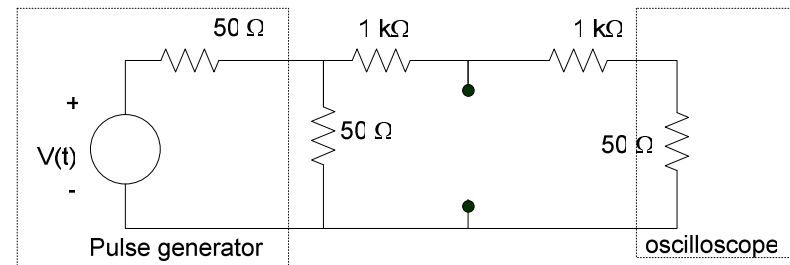
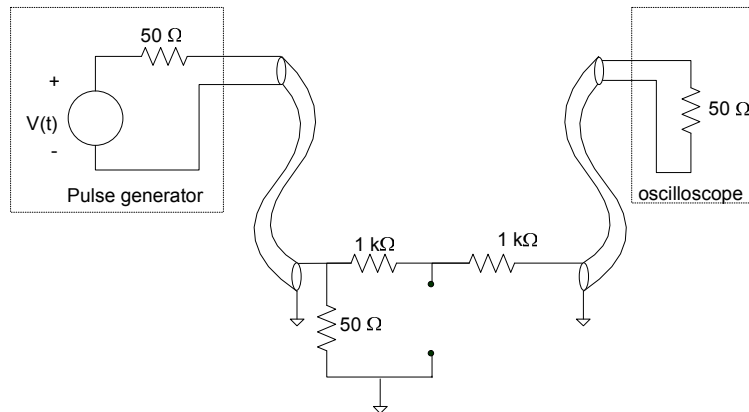


Ordinary capacitance

- Ex: measurement of a capacitance to ground, using a pulse source and an oscilloscope



Ordinary capacitance

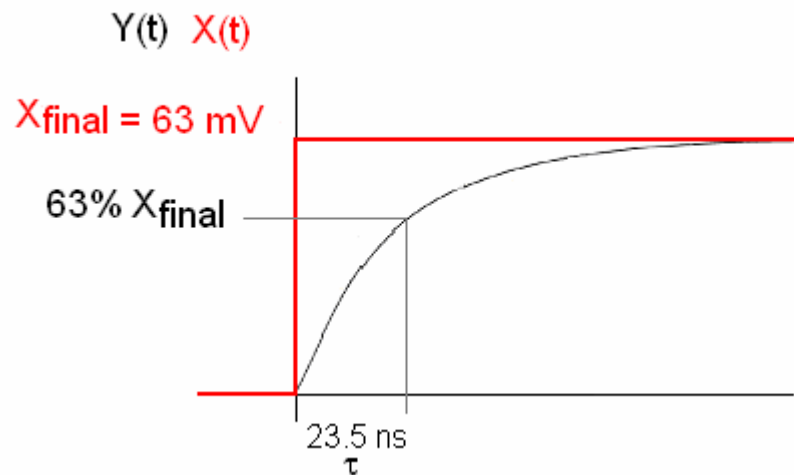


$$\tau = CR_{eq}$$

$$R_{eq} = [1000 + (50 // 50)] // (1000 + 50) = 518.7 \, \Omega$$

Ordinary capacitance

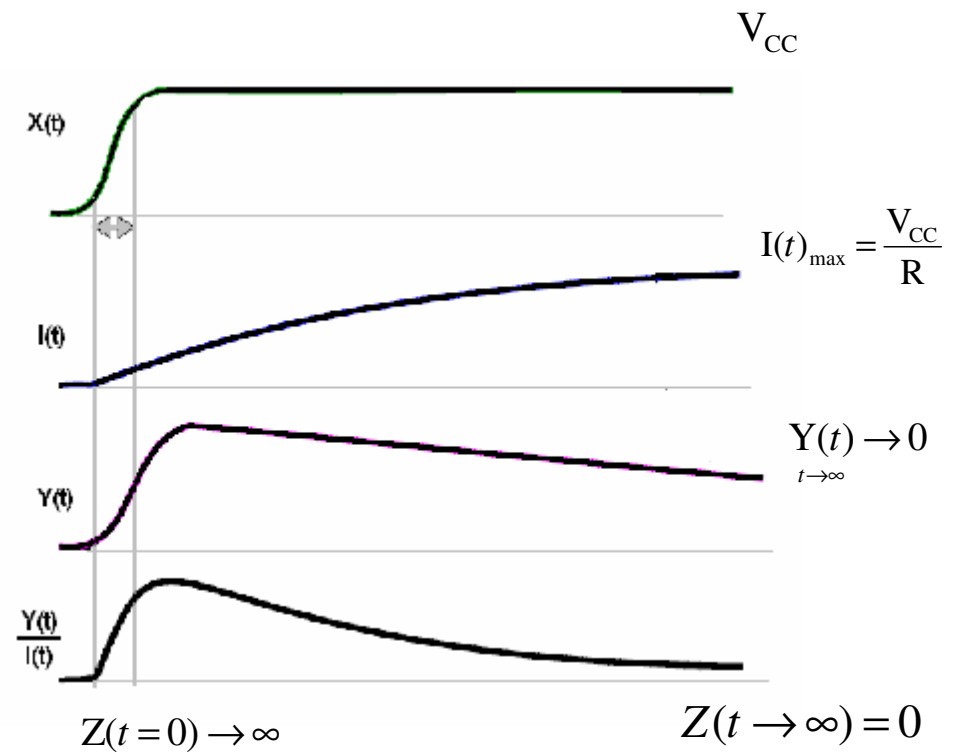
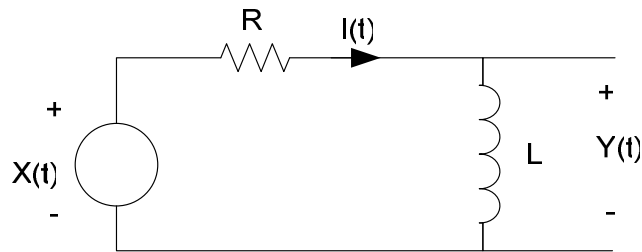
$$R_{eq} (measured) = 503 \, \Omega$$



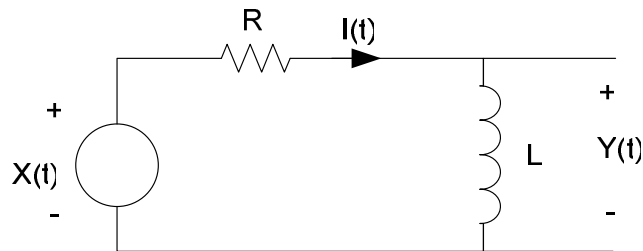
$$C = \frac{\tau}{R} = \frac{23.5 \text{ ns}}{503} = 46.7 \text{ pF}$$

Ordinary inductance

- Step response of a perfect inductor

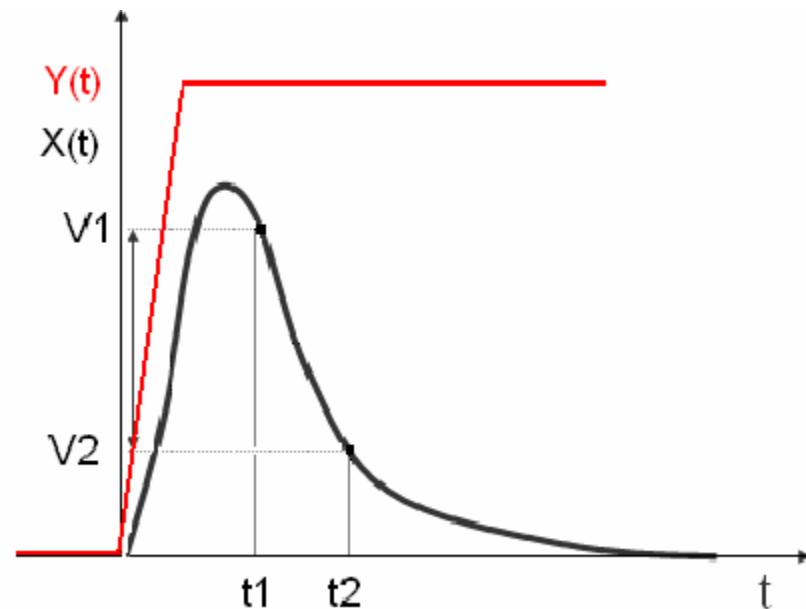


Ordinary inductance

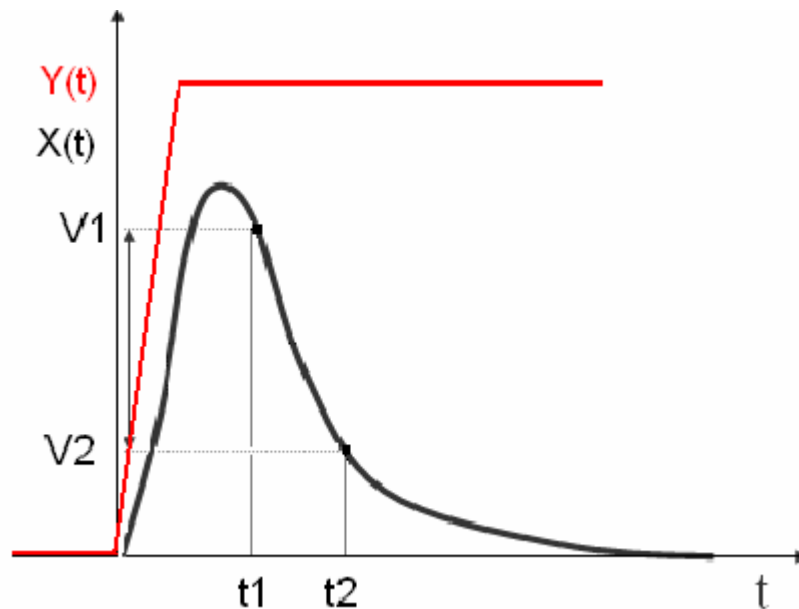


$$V_2 = 0.37 \times V_1$$

$$t_2 - t_1 = \tau$$



Ordinary inductance



$$\begin{cases} V_1 = V_{final} - (V_{final} - V_{initial})e^{-\frac{t_1}{\tau}} \\ V_2 = 0.37 \times V_1 = V_{final} - (V_{final} - V_{initial})e^{-\frac{t_2}{\tau}} \end{cases}$$

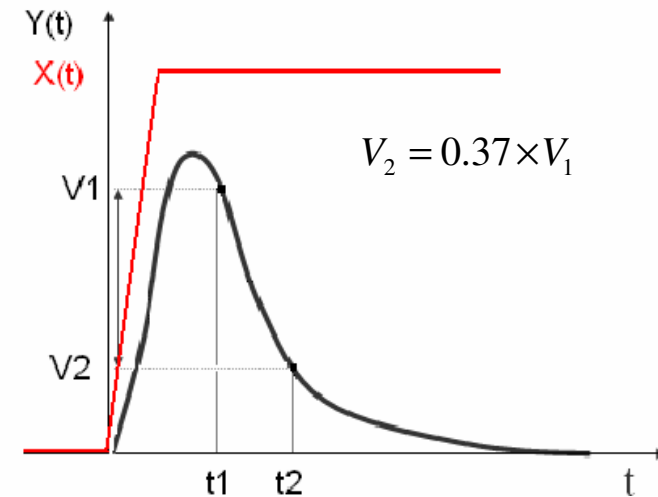
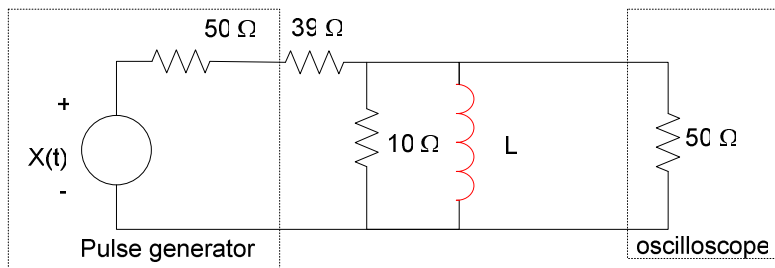
$$\begin{cases} V_1 = V_{initial} e^{-\frac{t_1}{\tau}} \\ 0.37 \times V_1 = V_{initial} e^{-\frac{t_2}{\tau}} \end{cases} \quad \frac{1}{0.37} = \frac{e^{-\frac{t_1}{\tau}}}{e^{-\frac{t_2}{\tau}}}$$

$$V(t_2) = 0.37V(t_1) \Rightarrow t_2 - t_1 = \tau$$

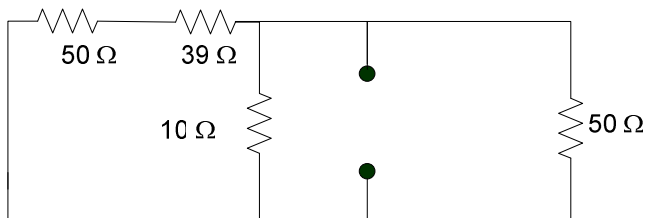
$$\tau = \frac{t_2 - t_1}{\ln 2.7} \approx t_2 - t_1$$

Ordinary inductance

- Ex: measurement of inductance to ground, using a pulse source and an oscilloscope.



- Time constant



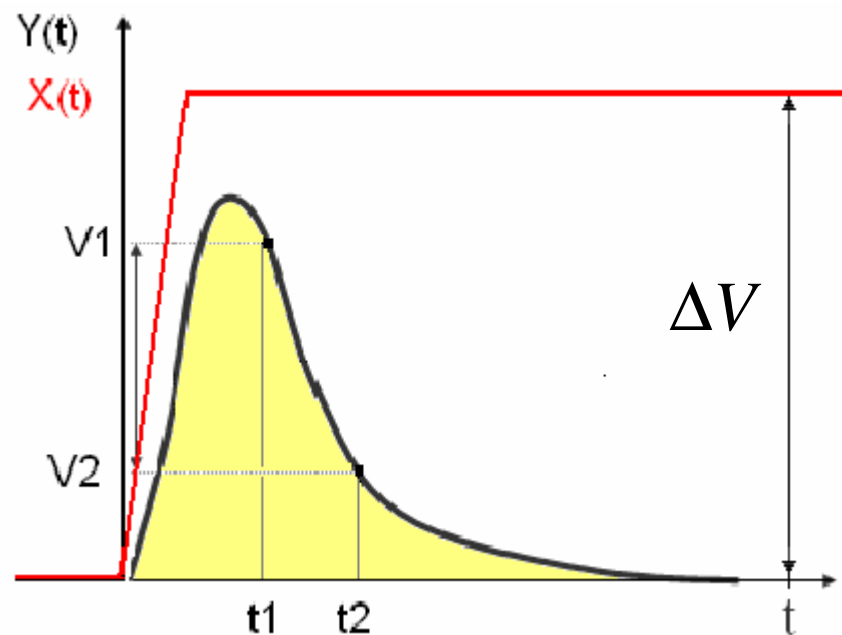
$$R_{eq} = [10 // (50 + 39)] // 50$$

$$\frac{L}{R_{eq}} = \tau \Leftrightarrow L = 1.4n \times 7.6 = 10.6nH$$

$$t_2 - t_1 \approx 1.4ns$$

Ordinary inductance

A better way to estimate the inductance



$$v(t) = L \frac{di(t)}{dt}$$

$$\int_0^{\infty} v(t) dt = L \int_0^{\infty} \frac{di(t)}{dt} dt$$

$$\int_0^{\infty} v(t) dt = L[i(\infty) - i(0)]$$

$$L = \frac{\text{area}}{i(\infty) - i(0)} = \frac{\text{area}}{\Delta i}$$

$$\Delta I = \frac{\Delta V}{R_s}$$

$$L = \frac{\text{Area} \times R_s}{\Delta V}$$

Mutual capacitance

- Mutual capacitance: wherever there are two circuits (two wires). Voltages in one circuit create electric fields that affect the other circuit. Mutual capacitance decay rapidly with distance.
- Mutual *capacitance* is represented by a parasitic capacitor (C_M) between the two circuits.
- A mutual capacitance injects a current I_M into circuit B proportional to the rate of change of voltage in circuit A (simple approximation).

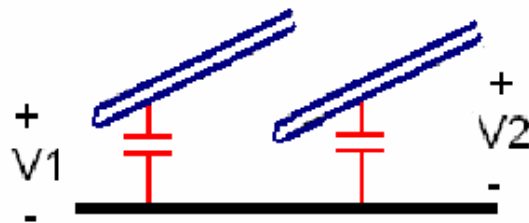
$$I_M = C_M \frac{dV_A}{dt}$$

- A more complete formula would use the difference in voltages between the two circuits and the effect of C_M load in both circuits.
- When the coupled noise voltage is less than 10% of the signal step size (on A), this approximation is accurate to one decimal place.

Mutual capacitance

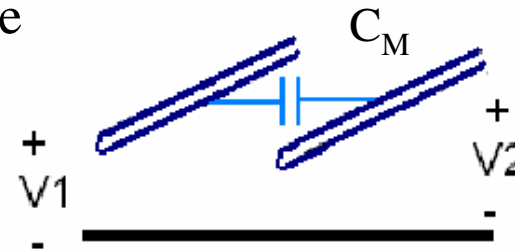
Ordinary capacitance versus mutual capacitance

- Between wire and ground

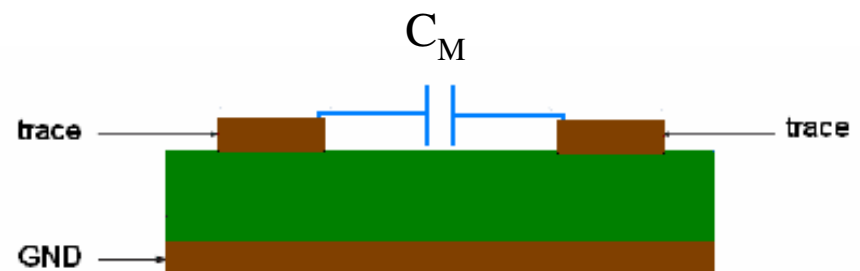
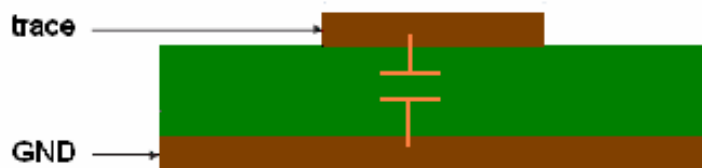


between two wires

cable

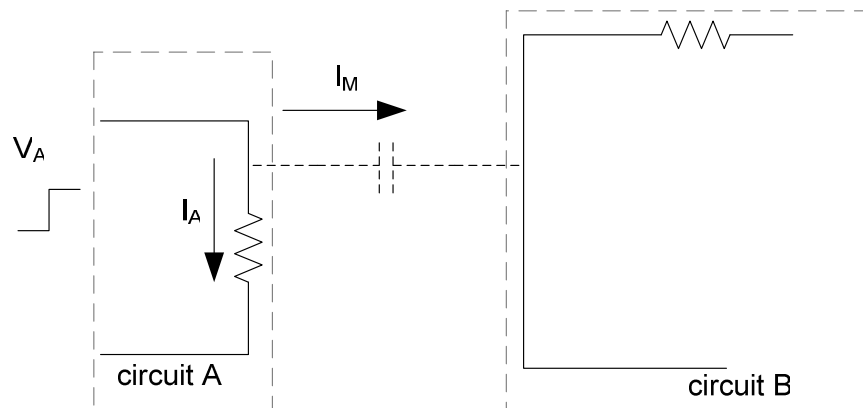


PCB



Mutual capacitance

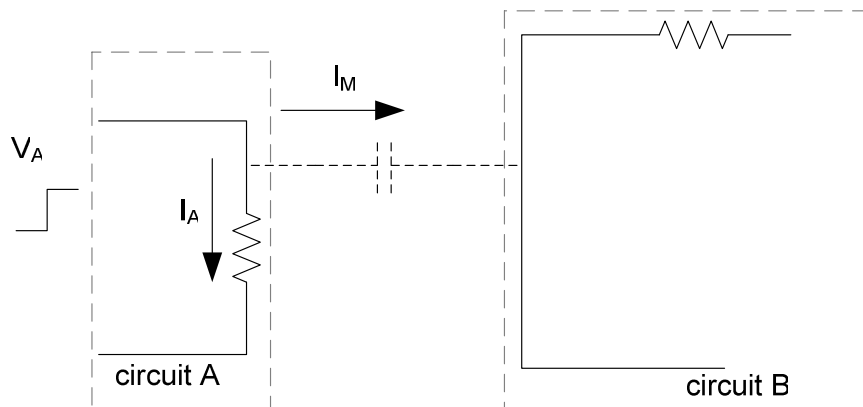
- Simple approach $I_M = C_M \frac{dV_A}{dt}$
 - The coupled current flowing in C_M is much smaller than the primary current in circuit A (C_M does not load circuit A).



$$I_M \ll I_A$$

Mutual capacitance

- Simple approach $I_M = C_M \frac{dV_A}{dt}$
 - The coupled signal voltage in circuit *B* is smaller than the signal in *A*



$$V_A \rightarrow I_M \rightarrow V_B$$

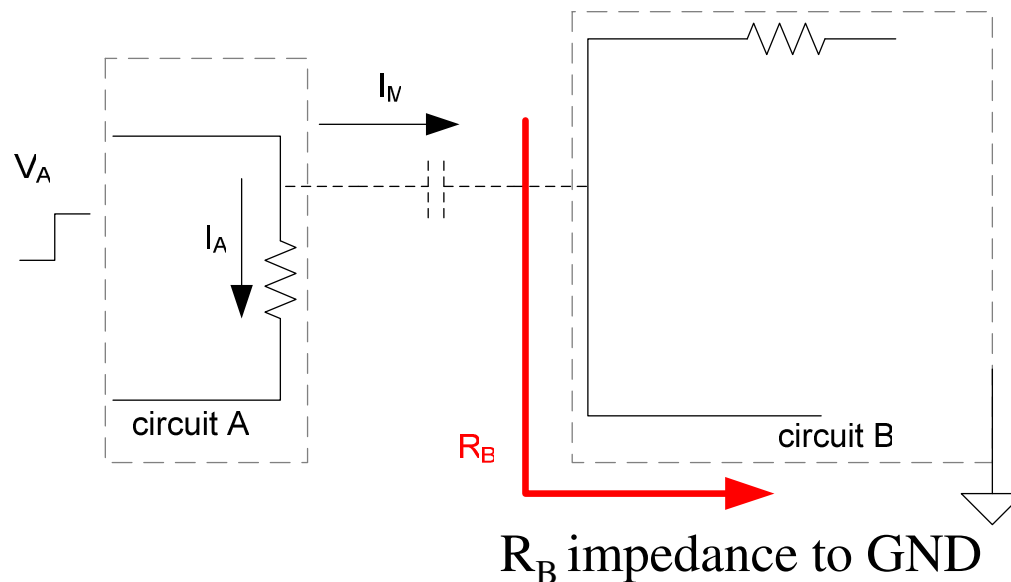
$$V_A \gg V_B$$

$$V_A - V_B \approx V_A$$

voltage difference between *A* and *B* is just V_A .

Mutual capacitance

- Simple approach $I_M = C_M \frac{dV_A}{dt}$
 - The mutual capacitance represents a large impedance compared to the impedance to ground of circuit B. Interactions between C_M and circuit B can be ignored.

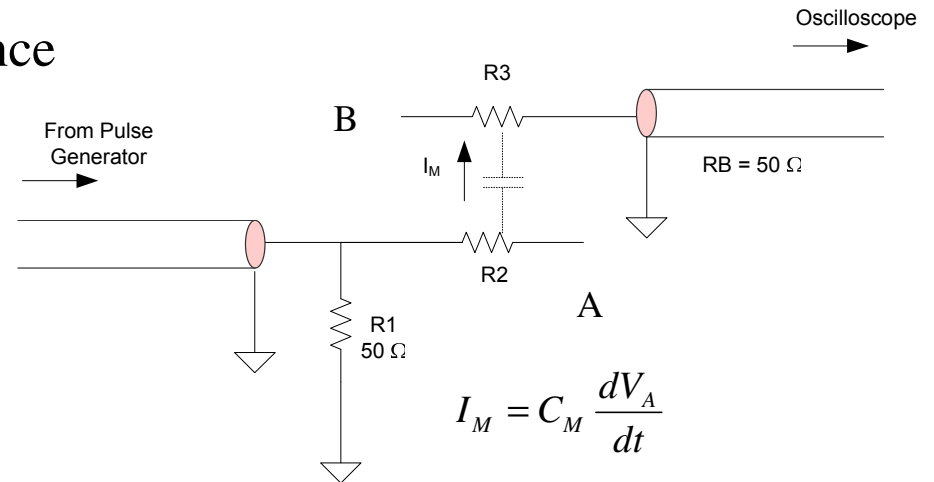
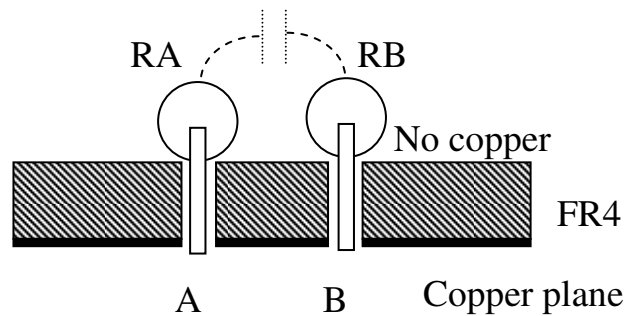


$$Z_M \gg R_B$$

$$V_B = R_B \times I_M$$

Mutual capacitance

- Ex: measurement of mutual capacitance



- Similar to inductance, measurement of mutual capacitance can be performed using area

$$\int_0^{\infty} R_B I_M dt = R_B C_M \int_0^{\infty} \frac{dV_A}{dt} dt$$

$$area = R_B C_M (V_A(0) - V_A(\infty)) = R_B C_M \Delta V_A$$

$$C_M = \frac{area}{R_B \times \Delta V_A}$$

Mutual capacitance

- Crosstalk: can be estimated as a fraction of V_A step.

- Coupled voltage in circuit B $I_M \times R_B$

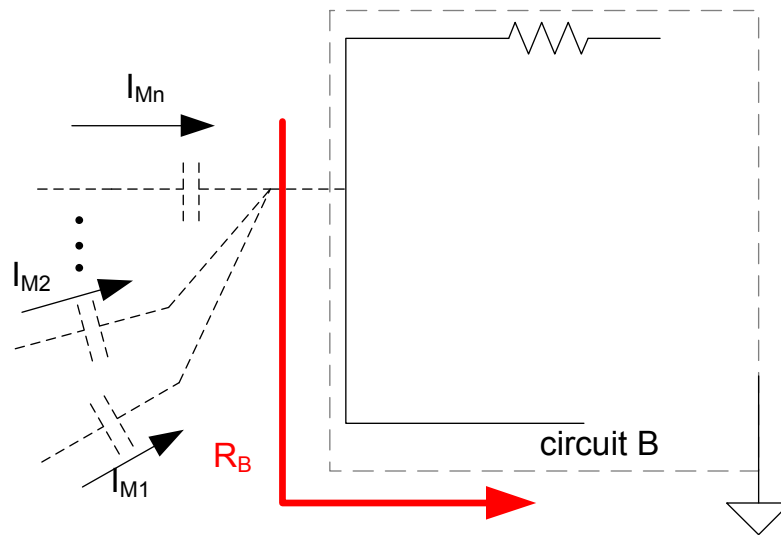
$$I_M = C_M \frac{dV_A}{dt}$$

- For a rise time T_r $\frac{dV_A}{dt} = \frac{\Delta V_A}{T_r}$

$$I_M = C_M \frac{\Delta V_A}{T_r} \quad \text{Crosstalk}(\%) = \frac{I_M \times R_B}{\Delta V_A} = \frac{R_B C_M}{T_r}$$

Mutual capacitance

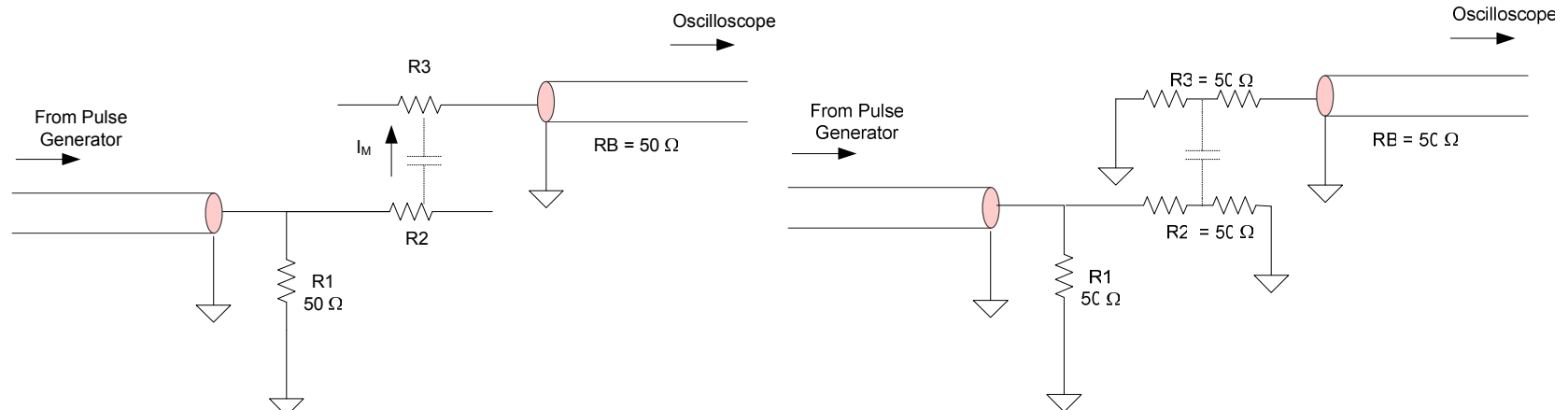
- For multiple interfering sources:
 - estimate the mutual capacitance for each pair
 - sum the fractional crosstalk from each source.



$$crosstalk_{total} = \sum_n crosstalk_n$$

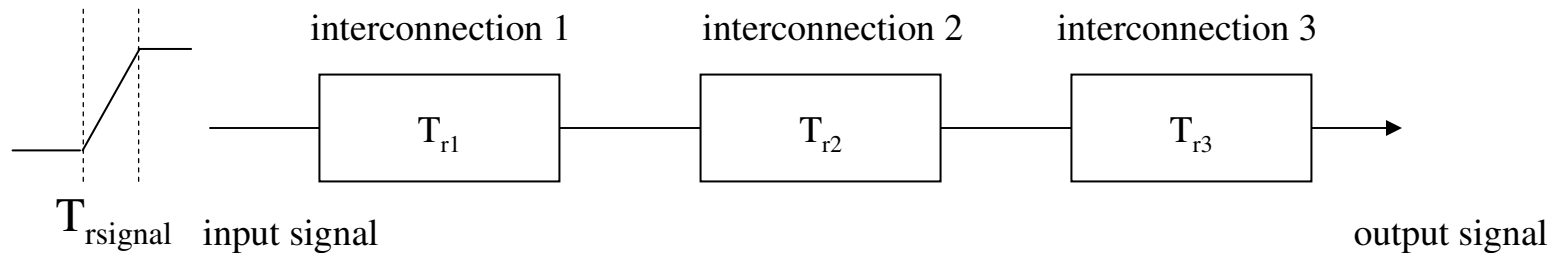
Mutual capacitance

R_2 and R_3 grounded on the other side: crosstalk reduced by a factor of 6



- V_A divided by 2 ($R_2/2$ in parallel with $R_2/2$)
- I_M : I_M to the probe is $(R_3 / 2)/(R_3+R_B)$ ($25/75 = 1/3$)
- Mutual capacitance can not be avoided in a small highly packed PCB. Therefore unused inputs should be connected to 1 or 0.

Revising last lecture



- T_{r1} , T_{r2} e T_{r3} :
 - intrinsic rise time of interconnections 1, 2 and 3
 - minimum rise time that the interconnection can transmit
- Determine the F_{knee} frequency of the output signal

$$F_{\text{knee}} = \frac{0.5}{\sqrt{T_{r\text{signal}}^2 + T_{r1}^2 + T_{r2}^2 + T_{r3}^2}}$$



Exercise

- Determine the rise time of an interconnection in order the increase of the rise time of a signal passing through the interconnection is less than 10%.

$$\frac{T_{rout}}{T_{rin}} = \frac{\sqrt{T_{rin}^2 + T_{r1}^2}}{T_{rin}} < 1.1$$

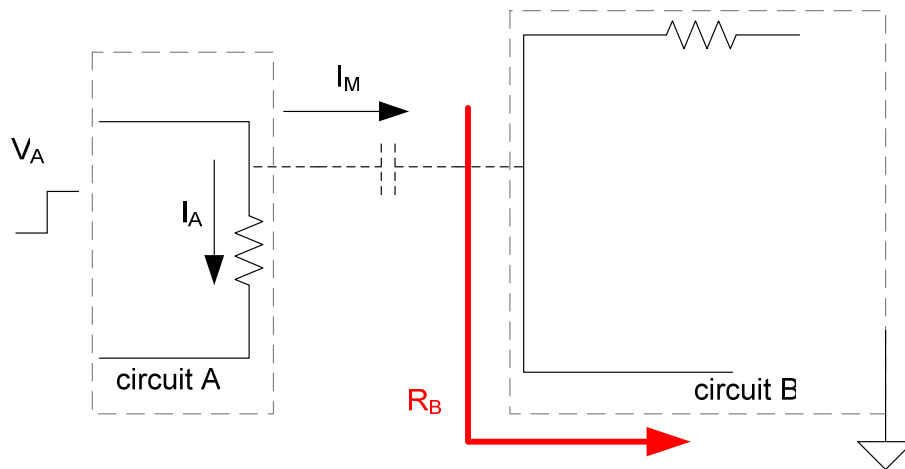
$$1 + \frac{T_{r1}^2}{T_{rin}^2} < 1.1^2$$

$$T_{r1} < 0.33 T_{rin}$$

- Rule of thumb T_r of the interconnection 50%
- BW of interconnection twice the Fnee of the signal

Revising last lecture

- How to identify resistive, capacitive and inductive behavior of a components based on the step response (with a pulse generator and an oscilloscope)?
- How to measure capacitance to ground based on the step response (with a pulse generator and an oscilloscope)?
- How to measure inductance to ground based on the step response (with a pulse generator and an oscilloscope)?
- What are the approximations to consider $I_M = C_M \frac{dV_A}{dt}$



$$I_M \ll I_A$$

$$V_A - V_B \approx V_A$$

$$Z_M \gg R_B$$



Revising last lecture

- When multiple circuits are generating crosstalk on a circuit B what is the total crosstalk on B?

$$crosstalk_{total} = \sum_n crosstalk_n$$

Lecture exercise

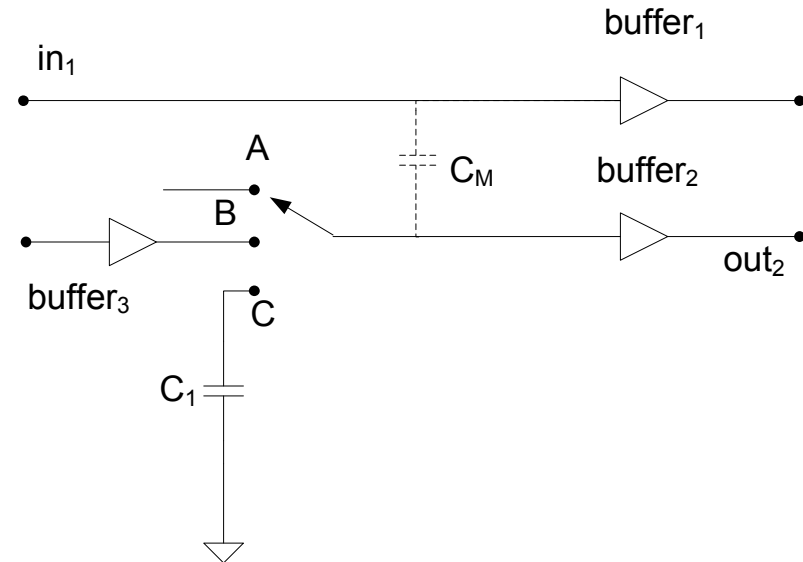
Buffers:

- noise margin $nm_H = nm_L = 0.4 \text{ V}$
- input impedance $R_{in} = 10 \text{ M}\Omega$
- output impedance $R_{out} = 100 \Omega$

Power supply $V_{CC} = 5 \text{ V}$

V_{in1} rise time T_r

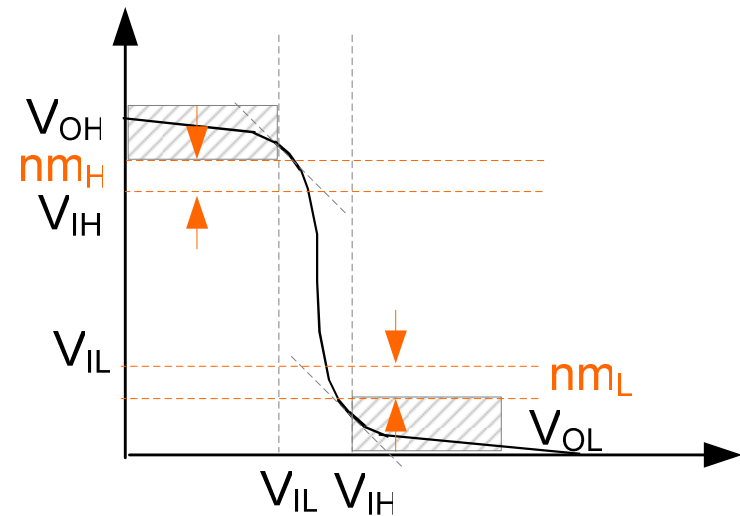
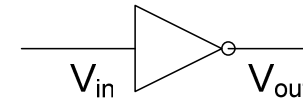
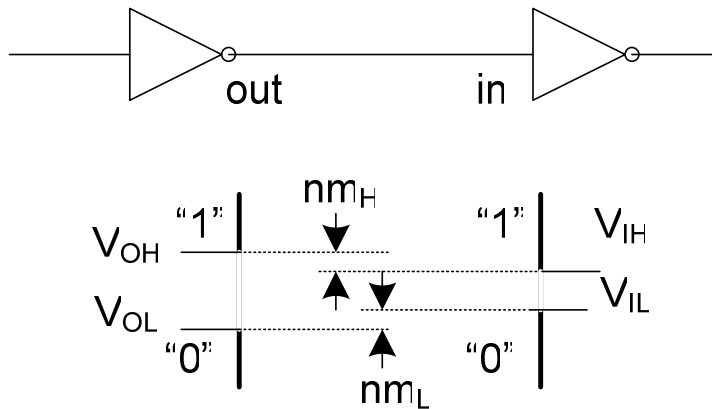
$CM = 0.5 \text{ pF}$



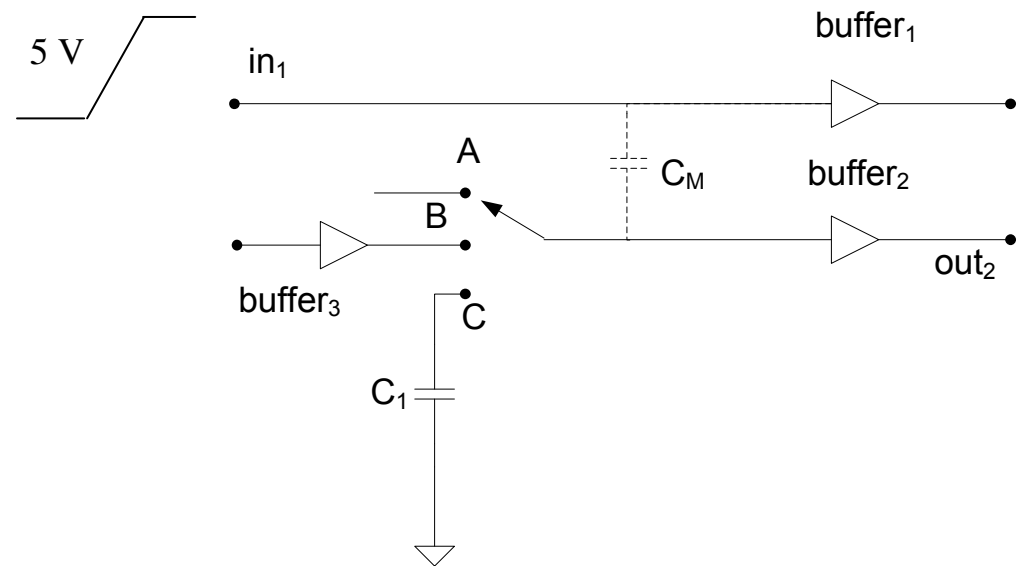
- Switch at position
 - Switch at position A: derive the cross talk relation between in_1 and out_2 .
 - Switch at position A: calculate the shortest T_r of V_{in1} that would not cause any noise at out_2 .
 - Switch at position B: calculate the shortest T_r of V_{in1} that would not cause any noise at out_2 .
 - Switch S is at position C and consider $T_r = 1 \text{ ns}$, calculate the minimum value of C_1 that any noise at out_2 .

Lecture exercise

- V_{IL} : maximum value recognized as a “0”
- V_{IH} : minimum value recognized as a “1”



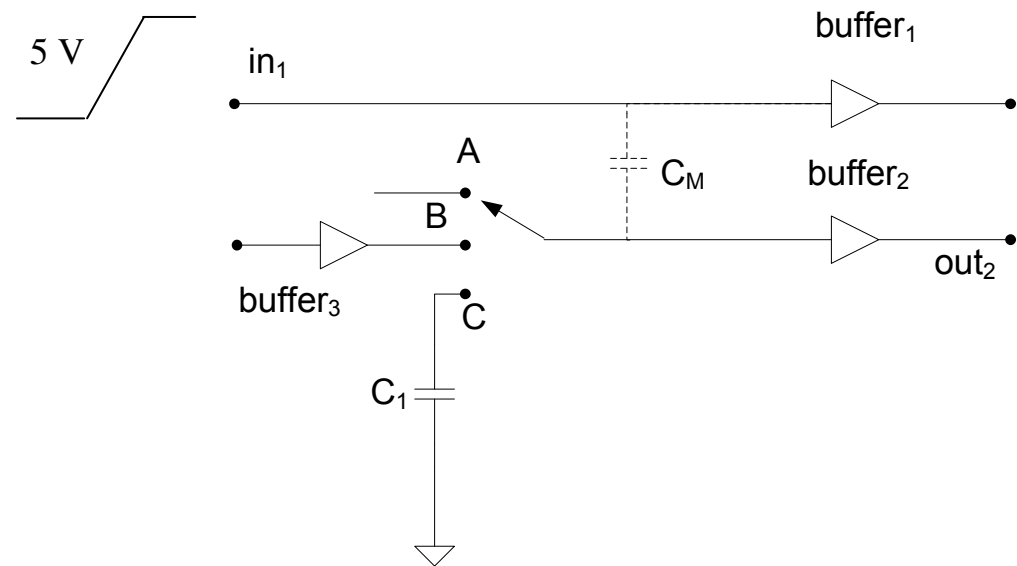
Lecture exercise



- Switch at position A: derive the cross talk relation between in₁ and out₂.

$$\text{Crosstalk}(\%) = C_M \frac{R_{in} \frac{\Delta V_{in1}}{T_r}}{\Delta V_{in1}} = \frac{C_M R_{in}}{T_r} = \frac{0.5p \times 10M}{T_r} = \frac{5 \times 10^{-6}}{T_r}$$

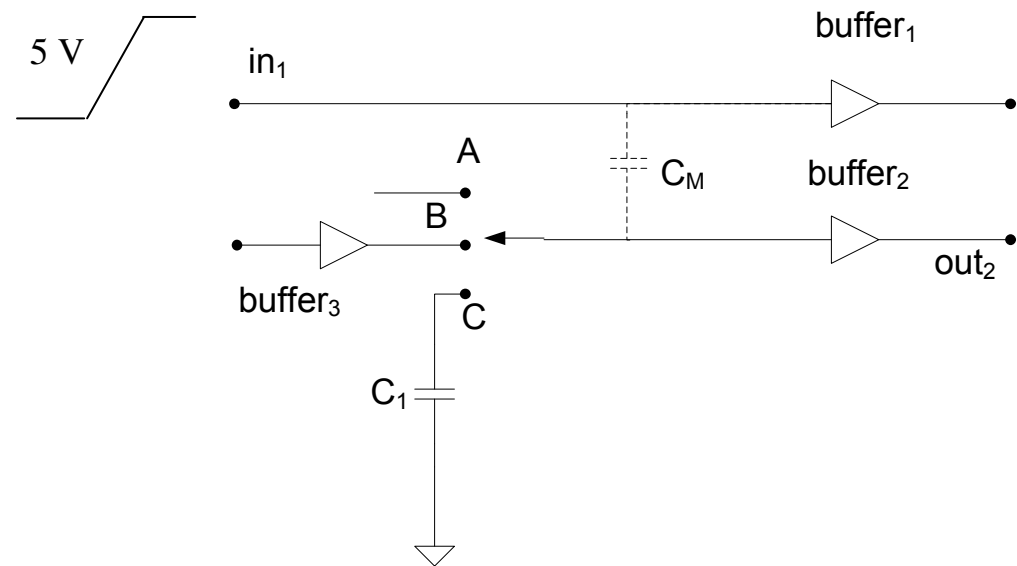
Lecture exercise



- Switch at position A: calculate the shortest T_r of V_{in1} that would not cause any noise at out₂.

$$0.4 > \frac{5 \times 10^{-6}}{T_r} \Delta V_{in} = \frac{5 \times 5 \times 10^{-6}}{0.4} \Rightarrow T_r > \frac{25 \times 10^{-6}}{0.4} = 62.5 \mu s$$

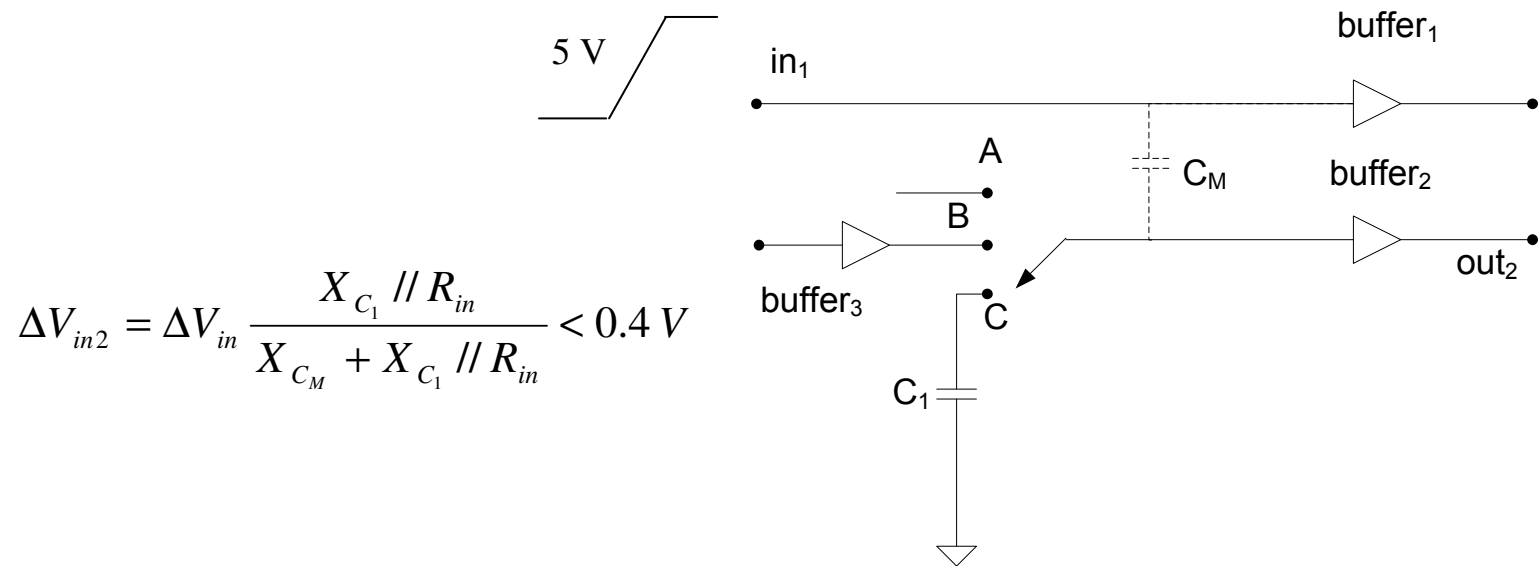
Lecture exercise



- Switch at position B: calculate the shortest T_r of V_{in1} that would not cause any noise at out_2 .

$$0.4 > \frac{0.5 p \times (10M // 100)}{T_r} 5 \Rightarrow T_r > \frac{250 \times 10^{-12}}{0.4} = 625 ps$$

Lecture exercise

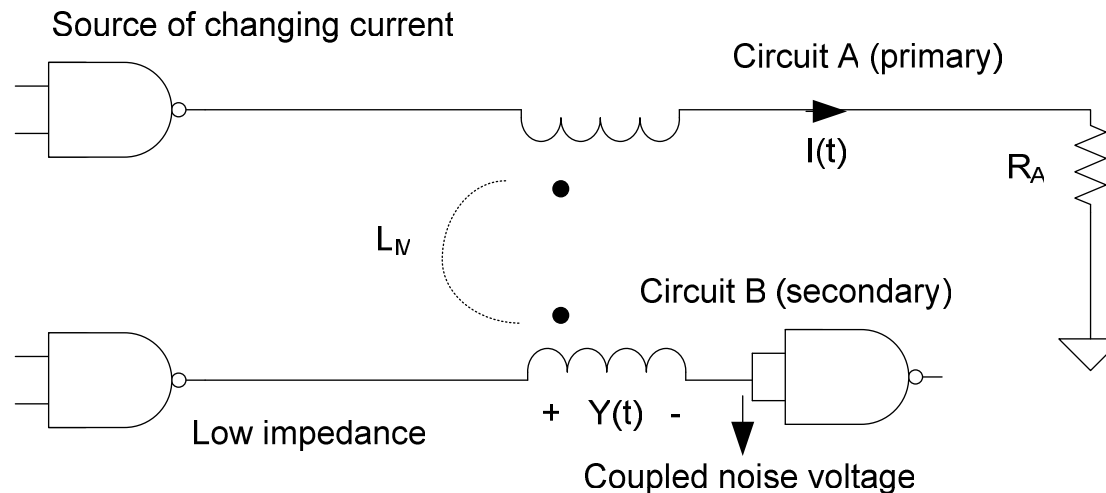


- Switch S is at position C and consider $T_r = 1\text{ns}$, calculate the minimum value of C_1 that would not cause any noise at out_2 .

$$|X_{C_M}| = \frac{1}{2\pi f_{knee} 0.5p} = \frac{T_r}{2\pi \times 0.5 \times 0.5p} = \frac{2n}{\pi p} = \frac{2 \times 10^3}{\pi} \quad |X_{C_1}| = \frac{1}{2\pi f_{knee} C_1} = \frac{10^{-9}}{\pi C_1}$$

Mutual inductance

- Mutual inductance: wherever there are two loops of current. The current in one loop creates a magnetic field that affects the second loop. Mutual capacitance decay rapidly with distance.
- Mutual inductive coupling between two circuits A and B acts as a tiny transformer connecting the circuits.





Mutual inductance

- A mutual inductance L_M injects a noise voltage Y into circuit B proportional to the rate of change in current in A (simple approximation).

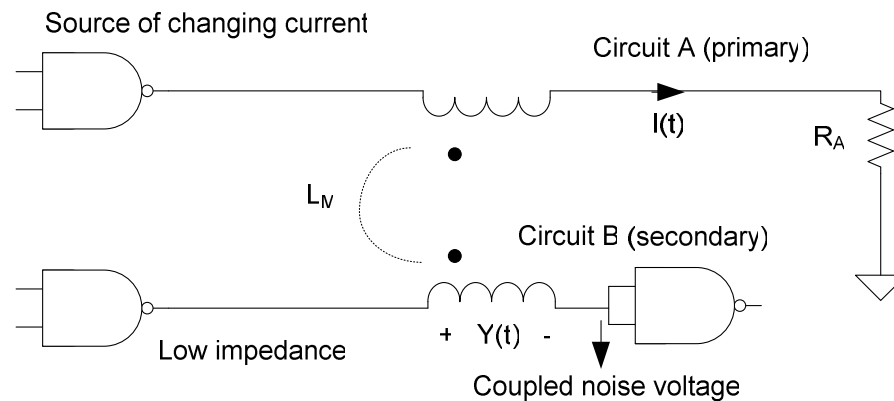
$$Y = L_M \frac{dI_A}{dt}$$

- Quick changes in circuit A induces large voltages in circuit B. Mutual inductance has great importance in high speed designs.
- A more complete formula would use the difference in currents between the two circuits and the loading of primary and secondary windings in both circuits.

Mutual inductance

- Simple approach

$$Y = L_M \frac{dI_A}{dt}$$



- Induced voltage across L_M is much smaller than the primary signal voltage (L_M does not load A).
- The coupled signal current in B is smaller than the current in A (I_A). Therefore, the small coupled current in B can be ignored and assume that the difference of currents in the coupling transform is I_A
- Secondary impedance is small compared to impedance to ground of B. Interactions between L_M and the secondary circuit can be ignored.

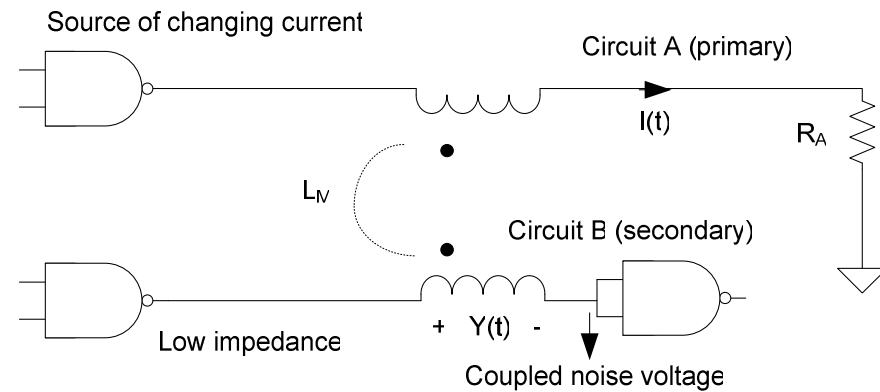
Mutual inductance

- Crosstalk can be estimated as a fraction of V_A .

$$\frac{dV_A}{dt} = \frac{\Delta V_A}{T_r}$$

$$\frac{dI_A}{dt} = \frac{1}{R_A} \frac{\Delta V_A}{T_r}$$

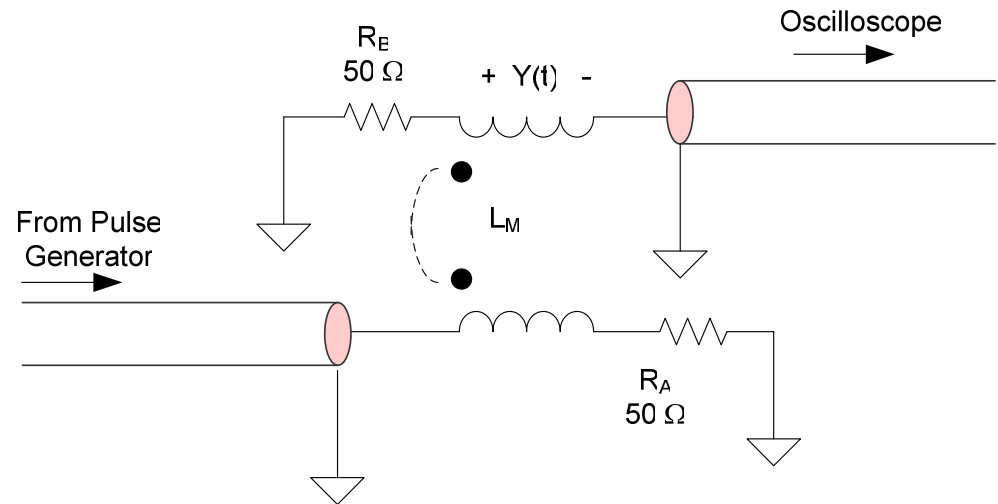
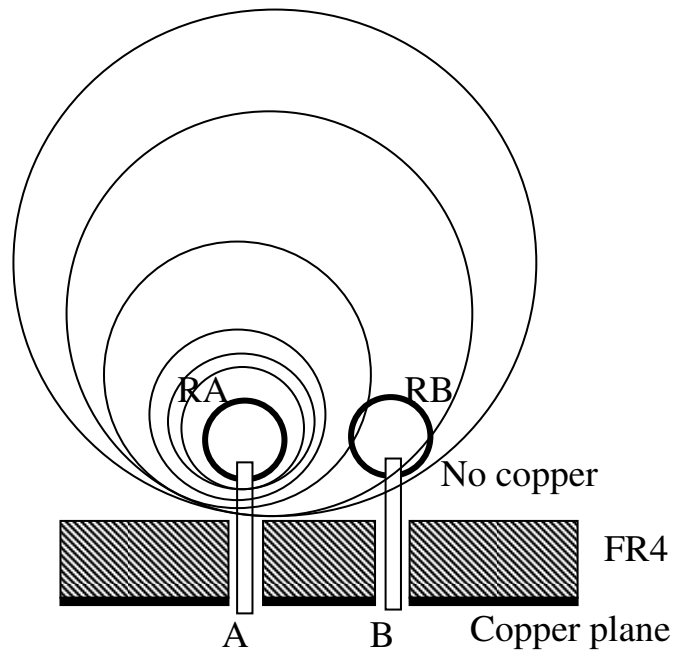
$$Y = L_M \frac{\Delta V_A}{R_A T_r}$$



$$\text{Crosstalk}(\%) = \frac{Y}{\Delta V_A} = \frac{L_M}{R_A \times T_r}$$

Mutual inductance

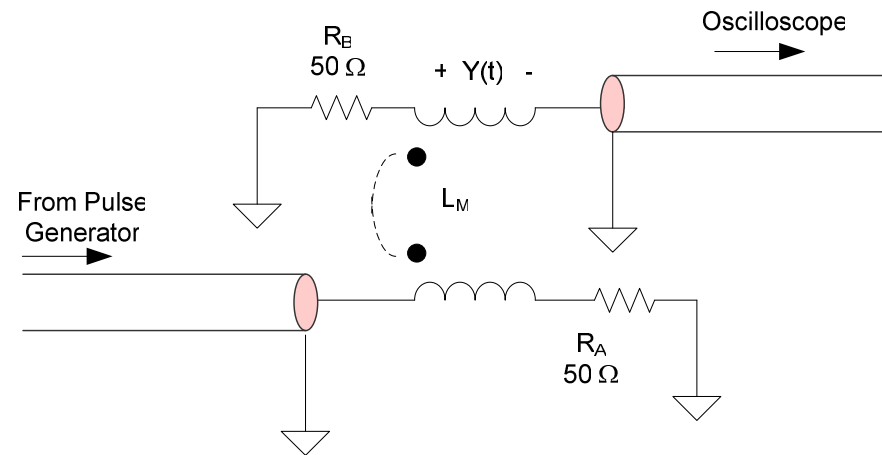
- Ex: measurement of mutual inductance between two traces



- Measurement of mutual inductance can be performed using area

Mutual inductance

$$Y = L_M \frac{dI_A}{dt}$$



- Measurement of mutual inductance can be performed using area

$$Y_{oscilloscope}(t) = \frac{1}{2} Y(t)$$

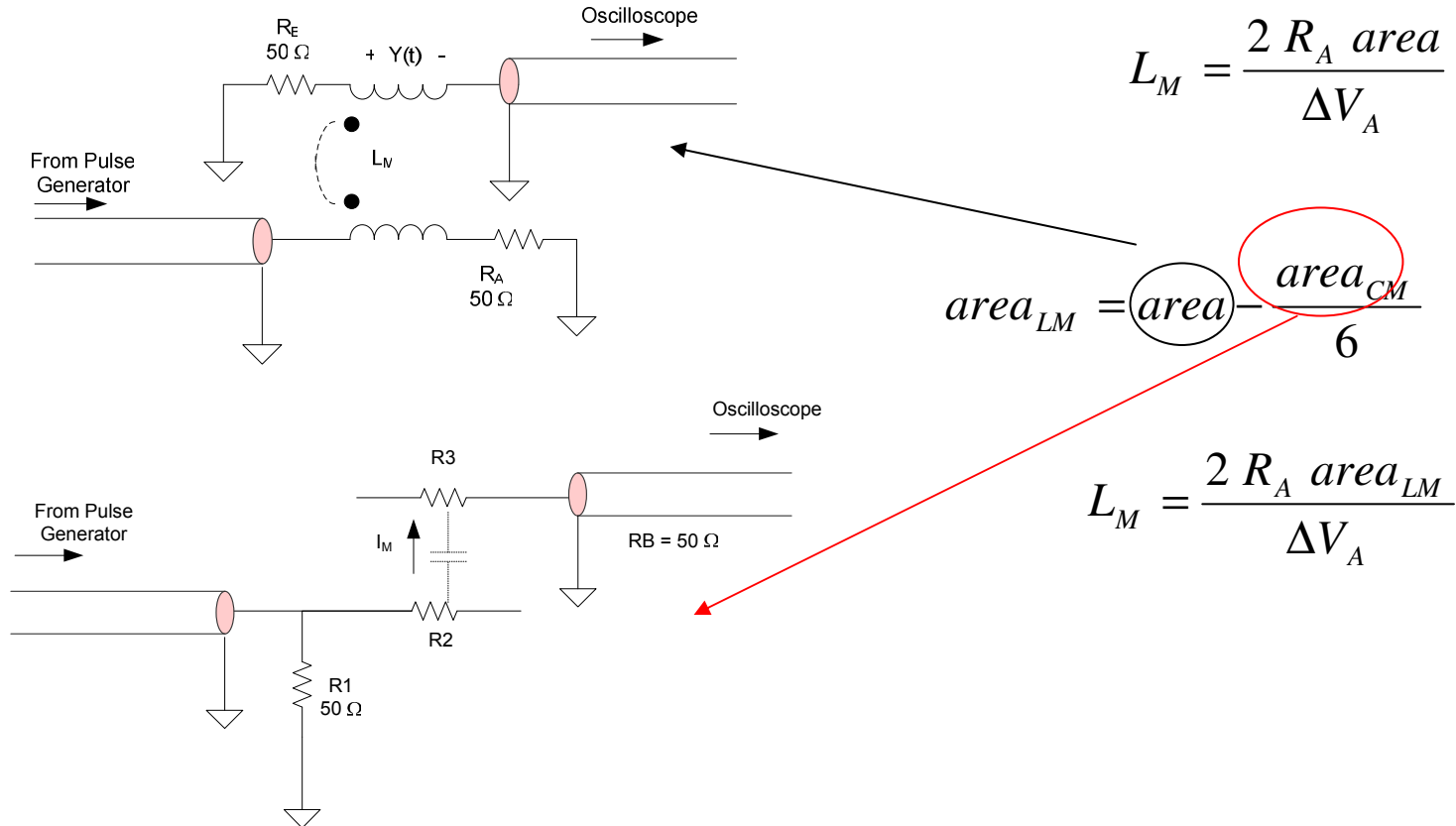
$$\int_0^{\infty} \frac{1}{2} Y(t) dt = \frac{1}{2} L_M \int_0^{\infty} \frac{dI_A}{dt} dt$$

$$area = \frac{1}{2} L_M [I_A(\infty) - I_A(0)] = \frac{1}{2} L_M \frac{\Delta V_A}{R_A}$$

$$L_M = \frac{2 R_A area}{\Delta V_A}$$

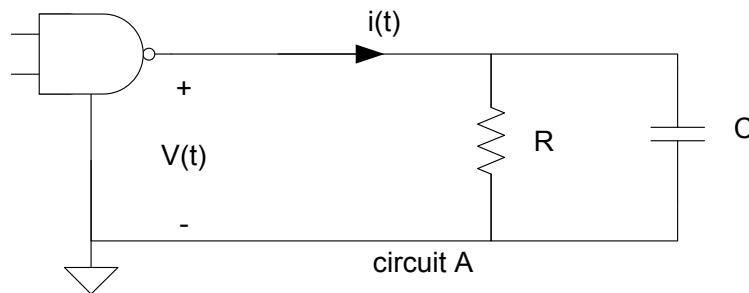
Mutual inductance

- More accurate measurement includes subtracting mutual capacitive interference



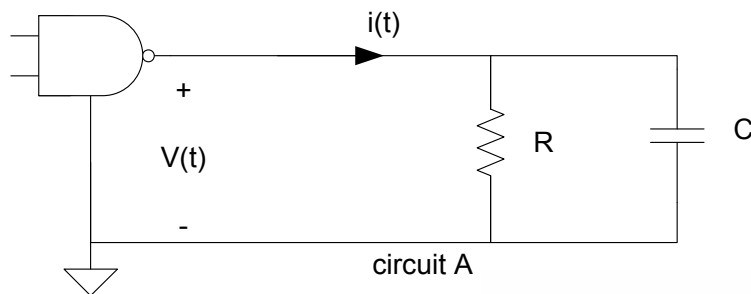
Mutual inductance versus mutual capacitance

- Among high speed digital circuits, mutual inductance is often a worst problem than mutual capacitance.



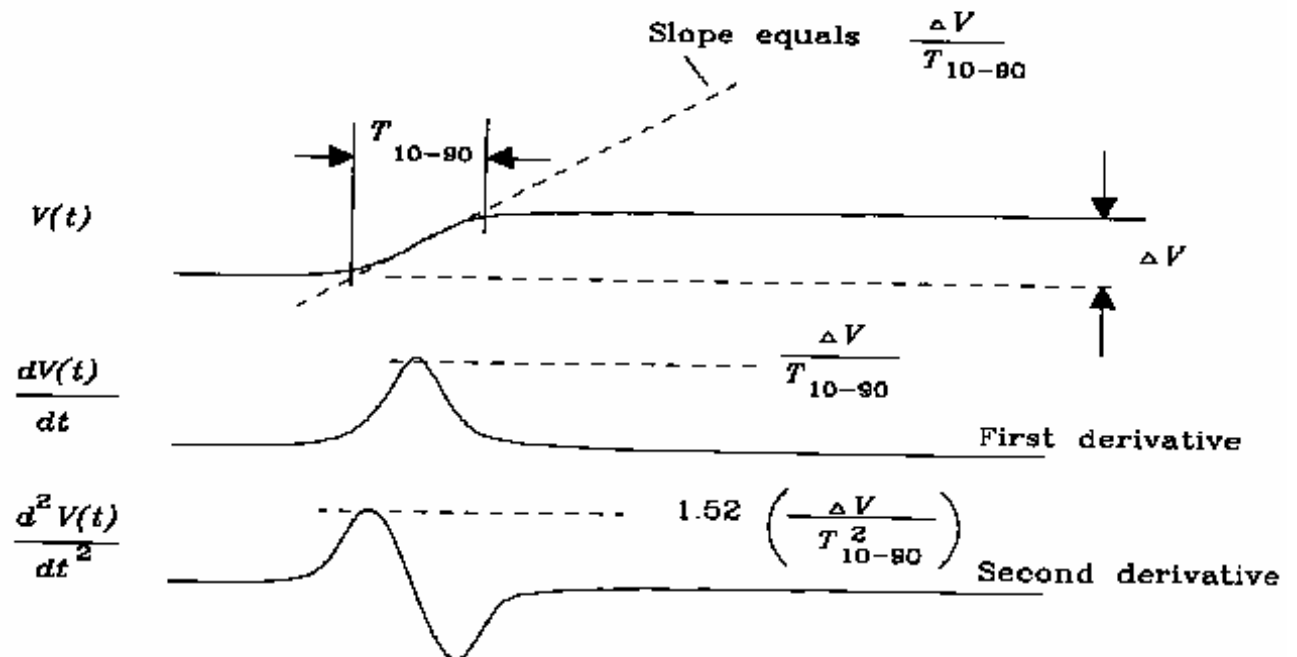
- Mutual capacitance effect on other circuits depending on: $\frac{dv(t)}{dt}$
- Mutual inductance effect on other circuits depending on: $\frac{di(t)}{dt}$

Mutual inductance versus mutual capacitance

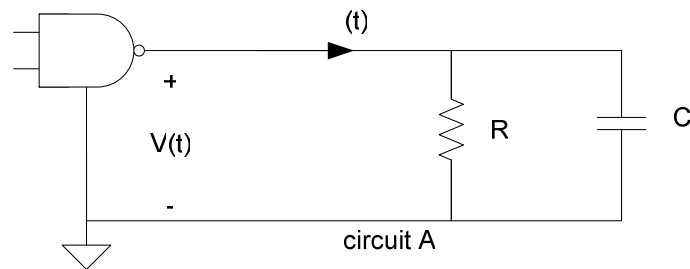


$$\frac{di(t)}{dt} = \frac{1}{R} \frac{dv(t)}{dt} + C \frac{d^2v(t)}{dt^2}$$

$$i(t) = \frac{v(t)}{R} + C \frac{dv(t)}{dt}$$



Mutual inductance versus mutual capacitance



$$\left. \frac{dv(t)}{dt} \right|_{\max} = \frac{\Delta V}{T_r}$$

$$\left. \frac{di(t)}{dt} \right|_{\max} = 1.52C \frac{\Delta V}{T_r^2}$$

- When we halve the rise time, we quadruple current variation with time (crosstalk).
- Interference is more serious for sharp changing edges (T_r is small).



Revising last lecture

- Mutual inductance:
 - Voltage Y injected by a circuit A into a circuit B (approximation):

$$Y = L_M \frac{dI_A}{dt}$$

- Circuit A (R_A)
Circuit B (R_B)
- $$\text{Crosstalk}(\%) = \frac{L_M}{R_A \times T_r}$$

- $$\text{crosstalk}_{total} = \sum_n \text{crosstalk}_n$$

Revising last lecture

- Transition at the output of a gate (RC load):
 - Mutual capacitance effect on other circuits depending on:

$$\left. \frac{dv(t)}{dt} \right|_{\max} = \frac{\Delta V}{T_r}$$

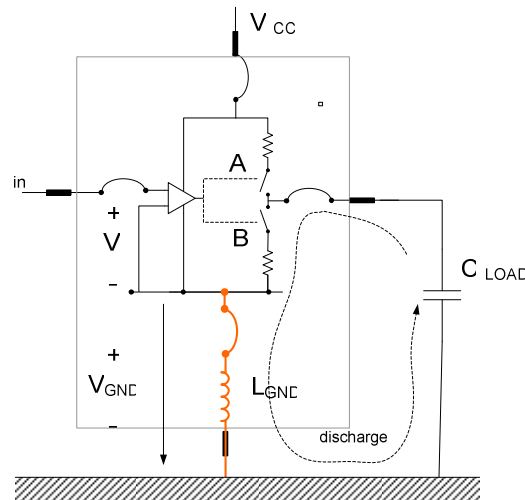
- Mutual inductance effect on other circuits depending on:

$$\left. \frac{di(t)}{dt} \right|_{\max} = 1.52C \frac{\Delta V}{T_r^2}$$

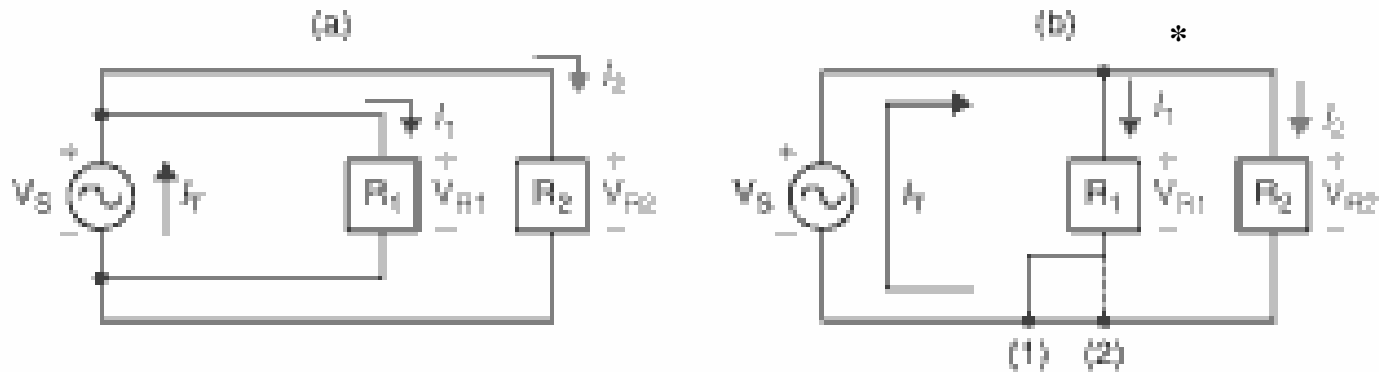
- Mutual inductance is often a worst problem than mutual capacitance

Ground Bounce

- Ground bounce is a transient voltage generated between two different points on the same return (ground) path, such as a package lead, a connector pin, different locations on the ground plane of a PCB:
 - Current flowing in the ground planes inducing voltage drops.
 - Current transients flowing in the ground leads of an IC package causing the ground rail of an IC to move with respect to ground on the PCB.



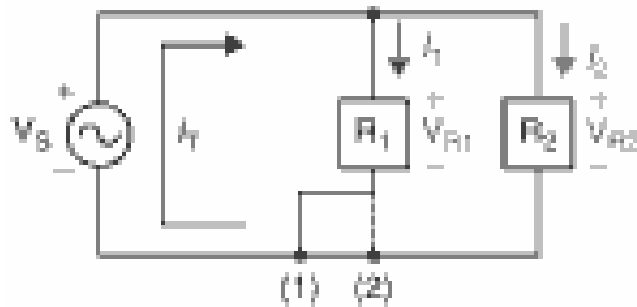
Ground Bounce



- Circuit (a): current flow in each branch is supplied and returns to the source through completely separated paths.
- Circuit (b): current flow in the two branches share a common ground
- Circuits (a) and (b) identical at schematic level (Kirchoff laws), but on the PCB can be significantly different.
- Circuit (b): connection at (1) or (2) can represent significant differences.

Figures from [5]

Ground Bounce



$$I_T = I_1 + I_2$$

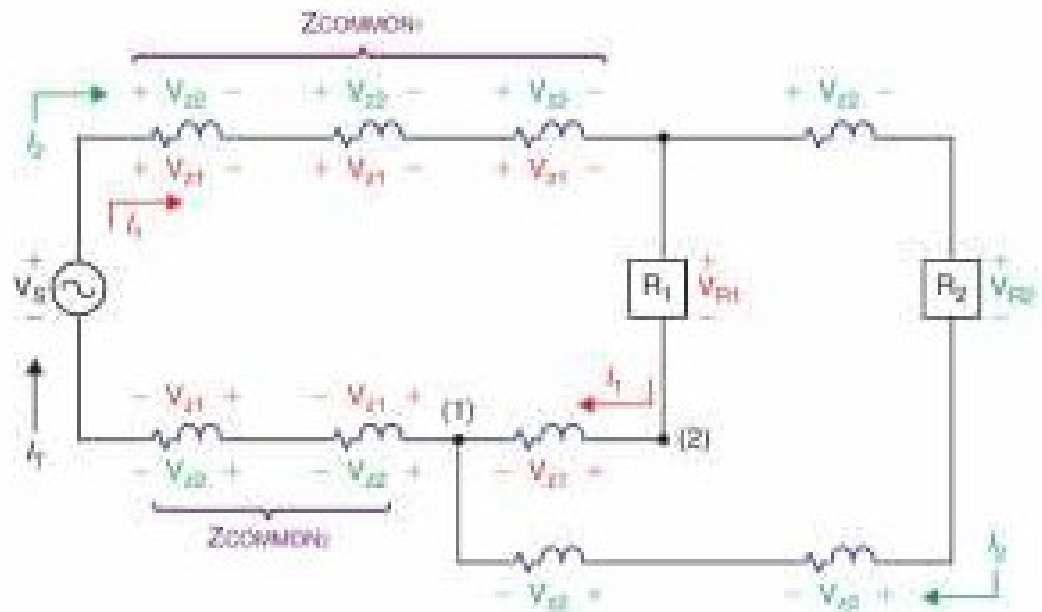
$$V_s = V_{R1} + V_{R2}$$

*

- The hidden schematic

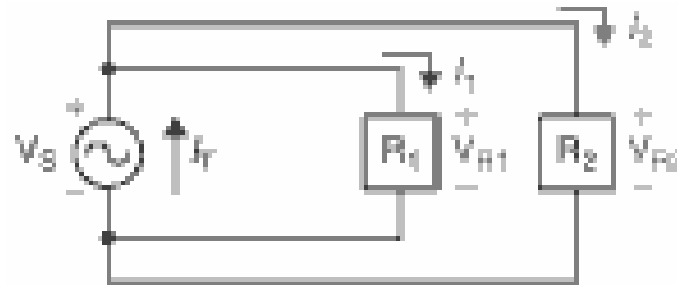
$$I_T = I_1 + I_2$$

$$V_s \neq V_{R1} \neq V_{R2}$$



Figures from [5]

Ground Bounce



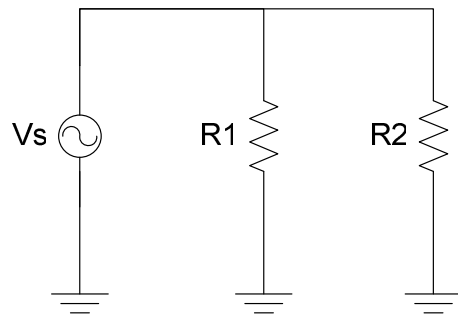
*

- Implementing routing with completely separate paths in high density PCBs is cumbersome

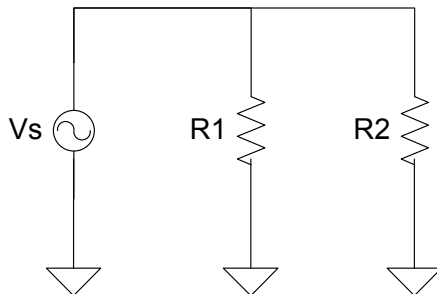
Figures from [5]

Ground Bounce

- Ground plane: in fact return plane. Unless return plane is physically connected to earth, it really has nothing to do with ground.
- We usually use the ground symbol, but

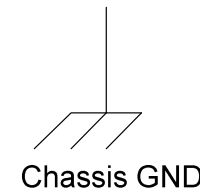
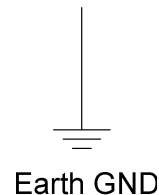
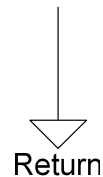


we want to indicate common return connections.



Ground Bounce

- IEEE/ANSI Standard Ground symbols



- Earth ground: A direct connection to earth, a direct connection to vehicle or airplane frames that serves the same function as earth ground.
- Return: used to indicate common return connections.
- Chassis GND: a connection to a chassis (physical frame or structure of a multi component device. May be completely different from earth ground.



Ground Bounce

- Bounce used to imply that the voltage on a node of a circuit moves with respect to some other node.
- If a transient voltage is generated on the return path, any signal paths that use this path as part of their return will see the transient ground bounce voltage as noise. The ground bounce voltage noise will appear on all signal lines that share the common return path.

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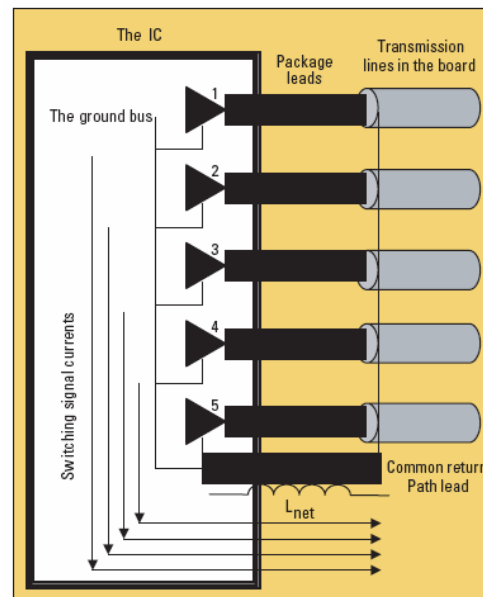


*Figure from [4]



Exercise

- Ground bounce is a form of crosstalk: it is not due to mutual inductance or mutual capacitance, but due to a shared return path.
- Consider an HCMOS circuit in a 20 pin DIP (20 pin DIP: 3.4 - 13.7 nH) with a ground pin inductance of 13.7nH. What is the value of ground bounce if one pin where a voltage switching edge of 2 ns drives a peak current of 20 mA?

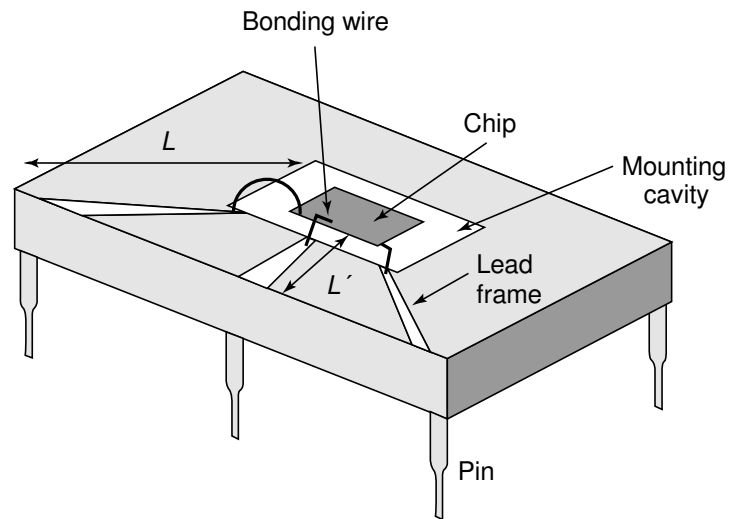
$$V = L \frac{di(t)}{dt} = 13.7n \frac{20m}{2n} = 137 \text{ mV}$$

- If 8 pins change simultaneously?

$$V' = 8 \times 137 \text{ mV} = 1.096 \text{ V}$$

Packaging

- Almost all packages suffer from problems with lead inductance and lead capacitance when used at high speeds.

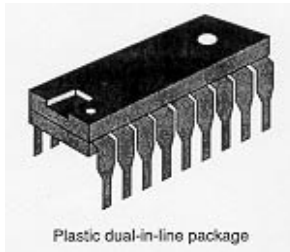


- Many types of packages:
Examples: <http://www.ti.com/sc/docs/package/guide.htm>

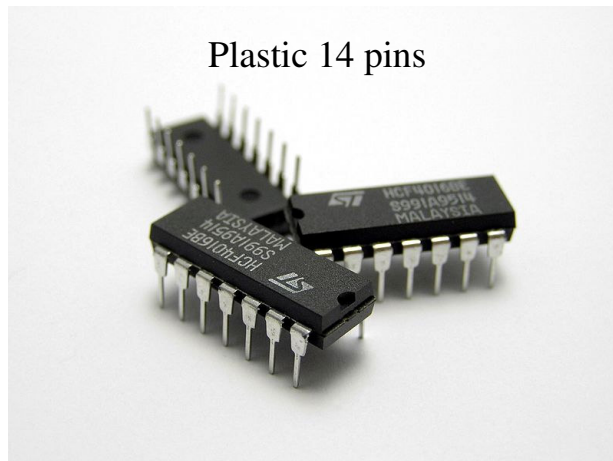
* Figure from bwrc.eecs.berkeley.edu/icbook/Slides/chapter9.ppt

Packaging

- DIP (dual in-line package)
 - leads penetrate the PCB surface



Plastic dual-in-line package



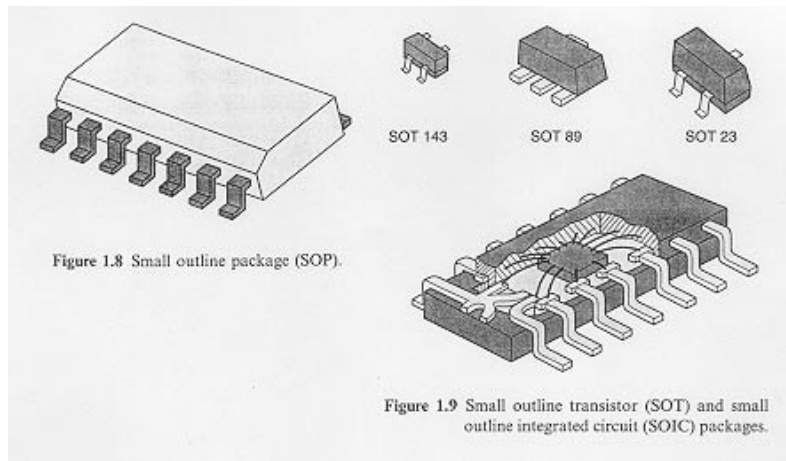
Plastic 14 pins



Ceramic DIP

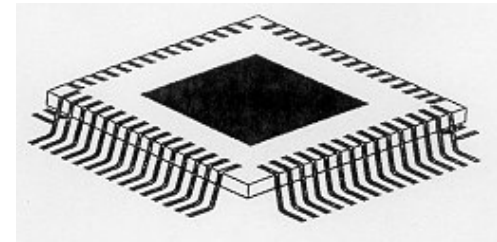
Packaging

- SMD (surface mount devices)
 - leads do not penetrate the PCB surface
 - ICs can be mounted on both sides for higher density



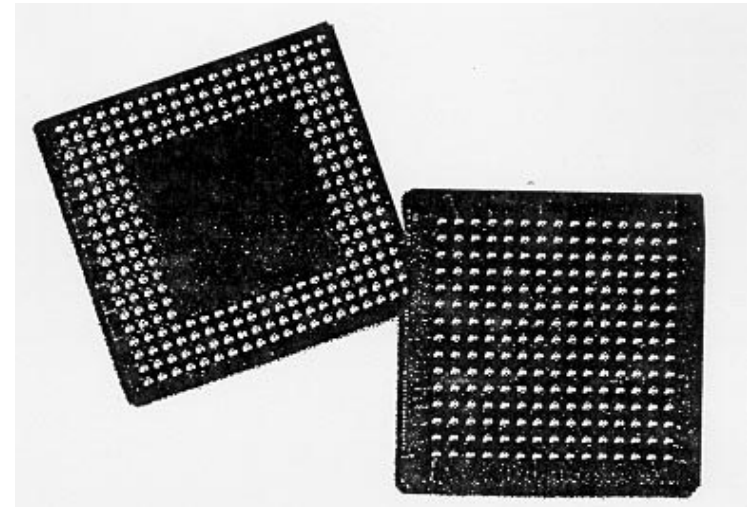
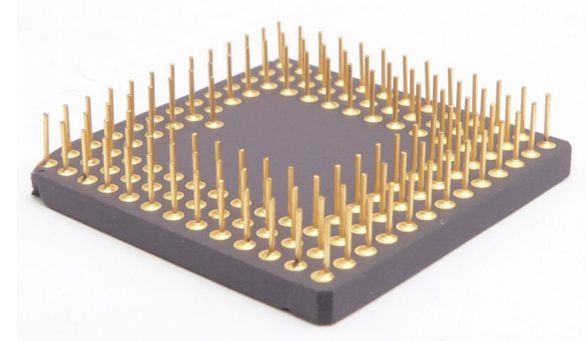
Packaging

- QFP (quad flatpacks)
 - plastic or ceramic bodies having leads on all 4 sides
 - SMT
- PLCC (Plastic Leaded Chip Carrier)
 - Surface mount technology (SMT) or PLCC sockets for true hole technology



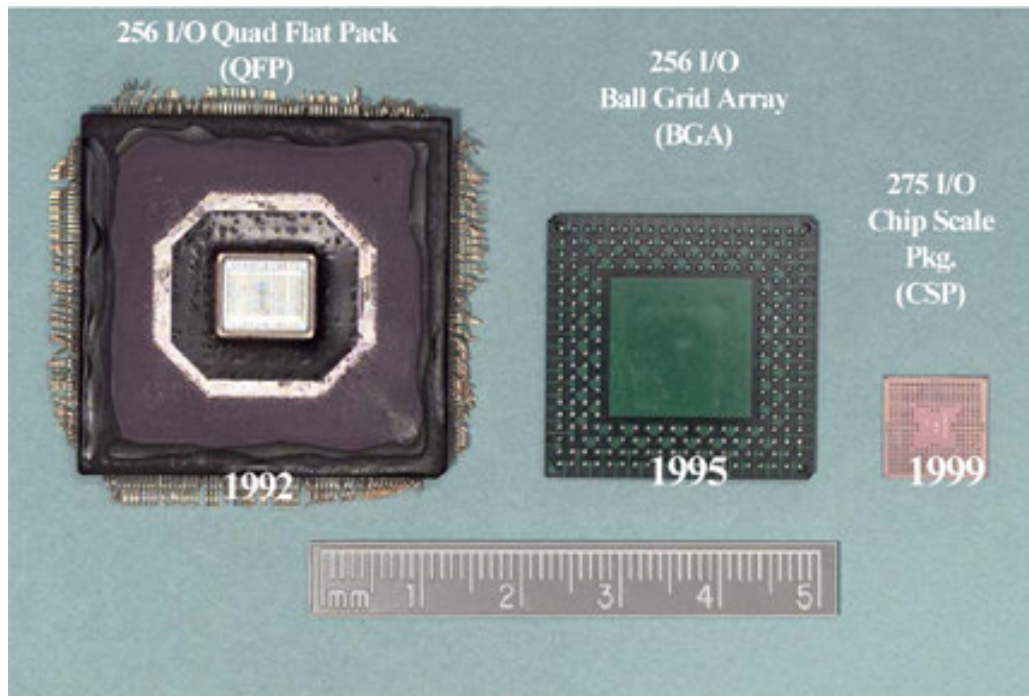
Packaging

- PGA (pin grid arrays)
 - Ceramic slab with one face covered, or partially covered, in a square array of metal pins
- BGA (ball grid arrays)
 - pins are replaced by balls of solder stuck to the bottom of the package



Packaging

- CSP (chip scale package): lower pitches than BGAs



http://nepp.nasa.gov/index_nasa.cfm/779/

Packaging

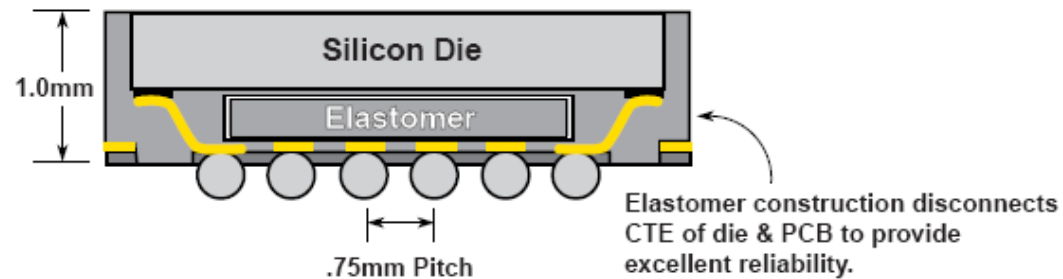
- CSP (chip scale package): stacked CSP and μ BGA



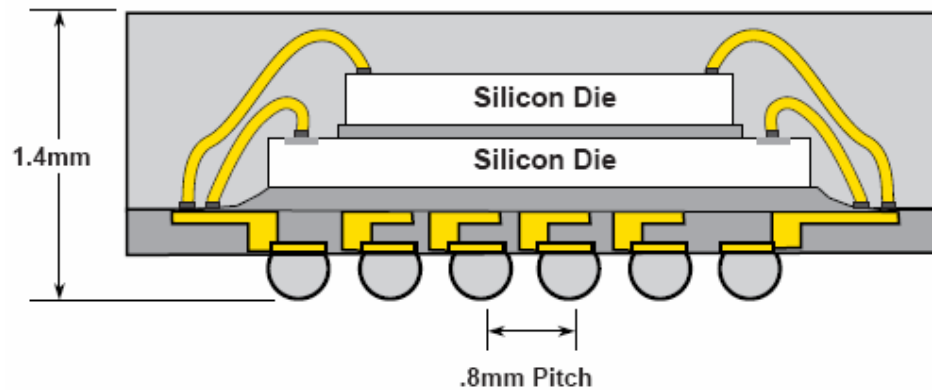
http://www.intel.com/design/packtech/CH_15.pdf

Packaging

- μ BGA



- Stacked CSP



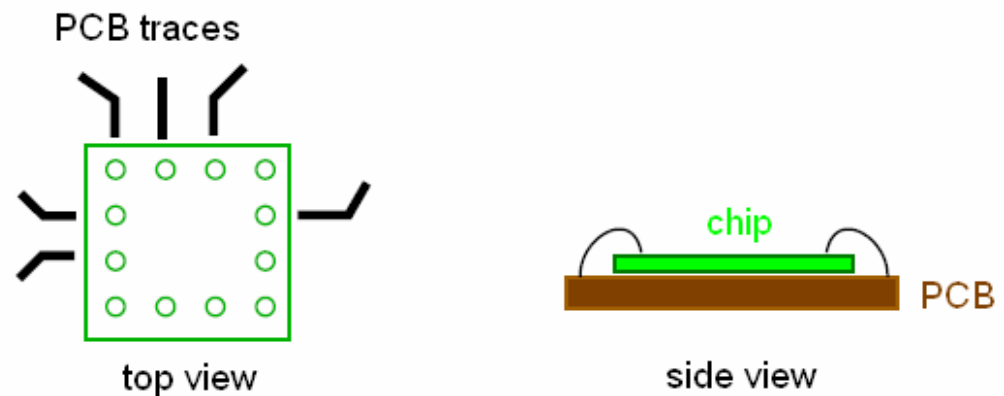
A75

http://www.intel.com/design/packtech/CH_15.pdf

Packaging

Packaging techniques to reduce lead inductance: special wire bond, tap automated bonding (TAB), flip-chip.

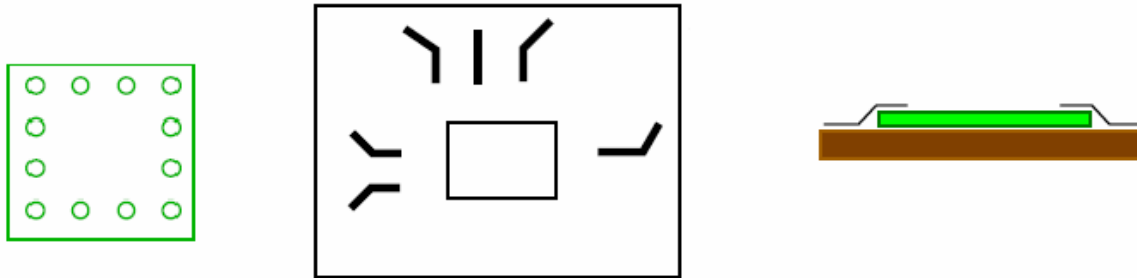
- special wire bond



- unsealed chip
- chip mounted face up
- wires connect PCB traces to chip pads
- result sealed with a blob of coating material or covered with a hermetically sealed lid over the entire circuit board

Packaging

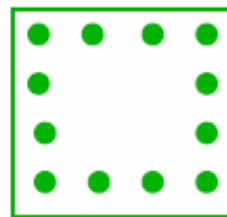
- tap automated bonding



- unsealed chip on a flex circuit
- chip mounted face up
- wires connect flex traces to chip pads and flex circuit traces to PCB
- result sealed with a blob of coating material or covered with a hermetically sealed lid over the entire circuit board

Packaging

- flip-chip



top view



side view

- Solder balls placed on each chip attachment pad
- Top side of the chip turned down onto the PCB mounting area and solder balls then re-melted .
- Good electrical behavior: bond length very small
- Mechanical and thermal problems: no mechanical compliance between chip and PCB requiring close match of thermal coefficients of expansion.

Packaging

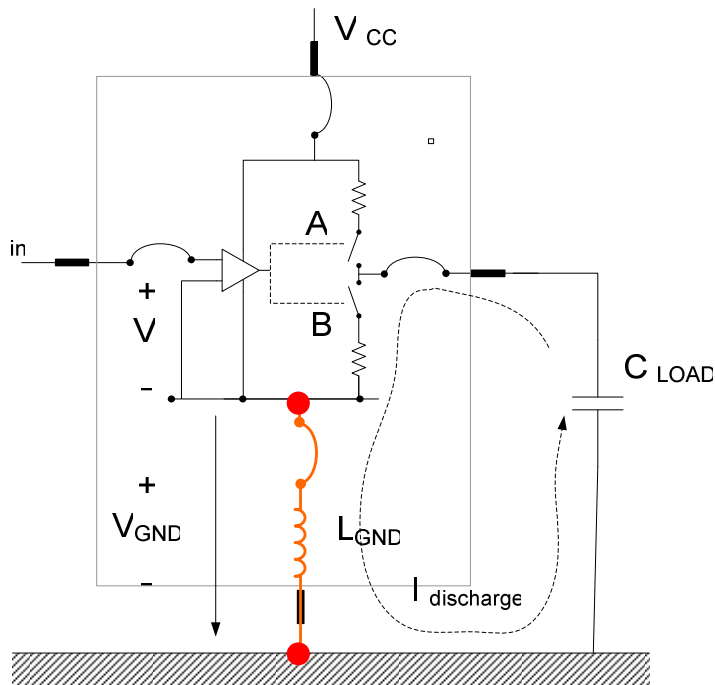
- Lead inductance and lead capacitance of some logic packages

14-pin plastic (DIP)	8nH	4pF
68-pin plastic (DIP)	35nH	7pF
surface mount PLCC	7nH	
wire bounded to hybrid substrate	1nH	1pF
Solder bump to hybrid substrate	0.1nH	0.5pF

- Ground lead inductance is a strong function of the package type.
- Larger packages have more lead inductance.
- Surface-mounted packages with shorter pins are less susceptible to this problem

Ground bounce

- Ground bounce: transient voltage generated between two different points on the same return path.



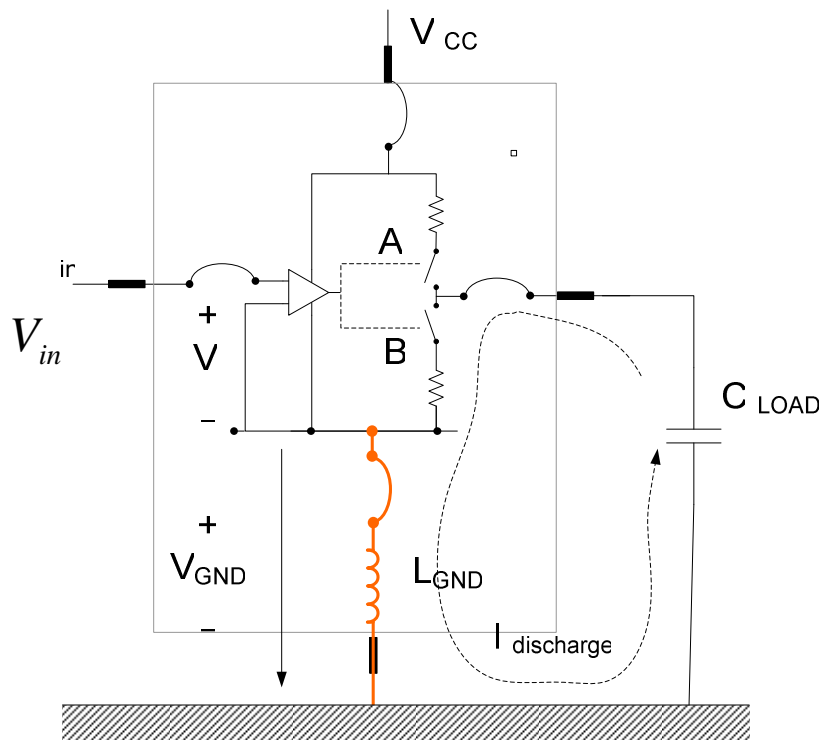
B closes: C discharges

$$V_{GND} = L_{GND} \frac{dI_{\text{discharge}}}{dt}$$

Ground bounce: variation on internal ground

Ground bounce

- V_{GND} is noise superimposed on the input



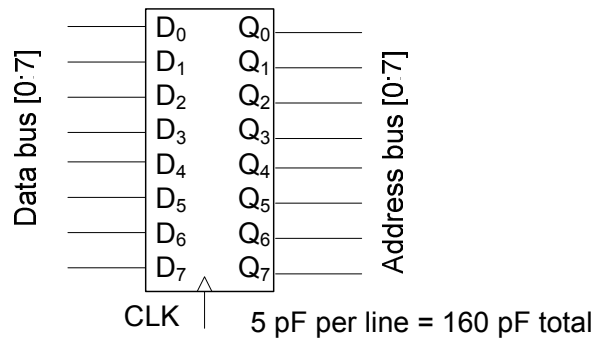
$$V_{out} = f(V_i)$$

$$V_i = V_{in} - V_{GND}$$

A rise in V_{GND} has the same effect that a fall in V_{in}

Ground bounce

- Ex: double clocking error
 - TTL octal D FF driving a bank of 32 memory chips (DIP package)



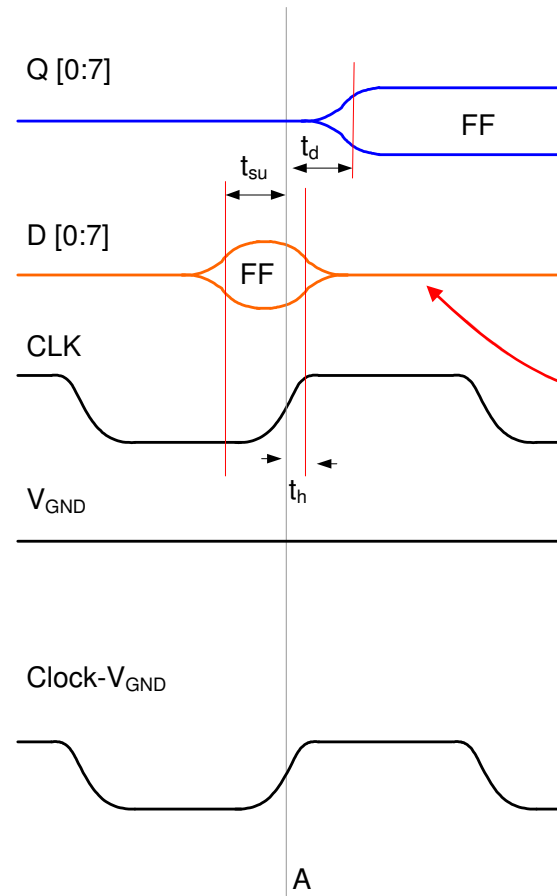
t_{su} – setup time (3ns)

t_h – hold time (1 ns)

t_d – gate propagation delay (3 ns)

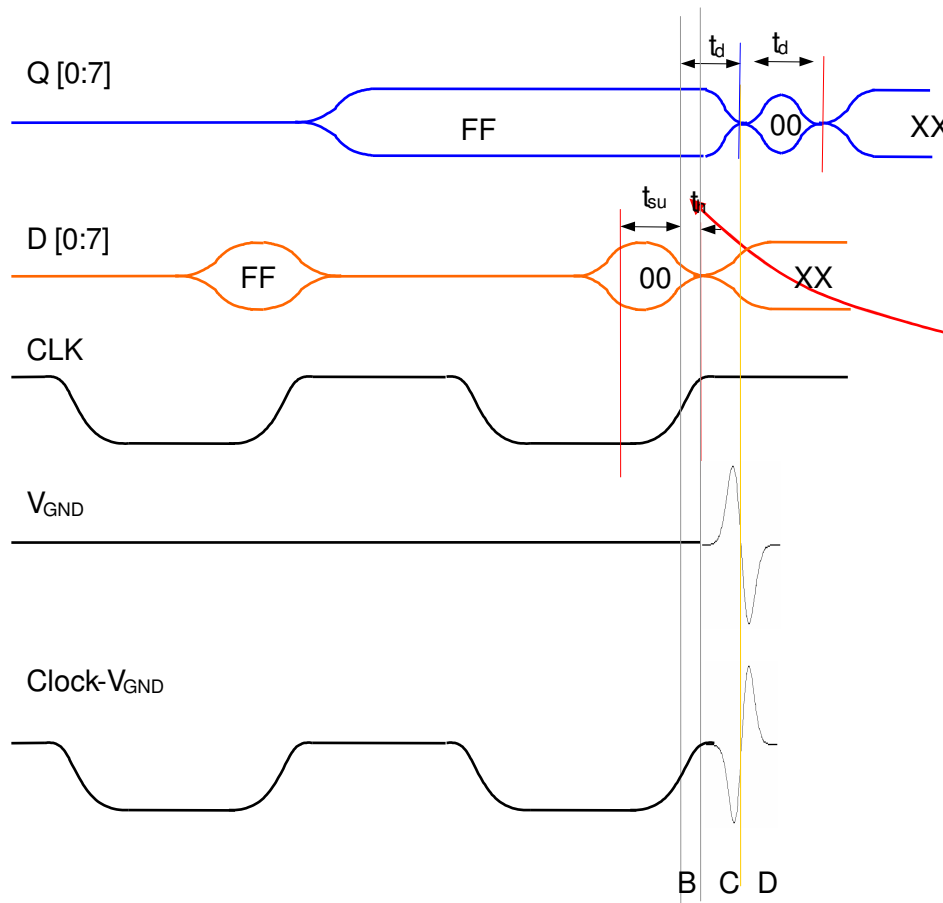
Ground bounce

$D[0:7] = FF$



Ground bounce

$D[0:7] = FF \rightarrow D[0:7] = 00$



$t = t_D \Rightarrow FF \rightarrow 00$

erroneous data latched

Exercise

- Four signal lines in a integrated circuit share the same return lead. The total impedance environment is 50Ω and a total inductance for the return or ground lead is 2 nH. The rise time of the signal is 0.5 ns. Determine the relative ground bounce.

$$T_r = 5 \text{ ns} \quad L = 2 \text{ nH} \quad Z_o = 50 \Omega \quad n = 4 \quad V_{gb} = n \times L \times \frac{dI}{dt}$$

$$V_{gb} = n \times L_{net} \times \frac{\frac{\Delta V_a}{Z_o}}{T_r} \quad \frac{V_{gb}}{\Delta V_a} = \frac{n \times L}{T_r \times Z_o} = \frac{4 \times 2n}{0.5n \times 50} = 32\%$$

Exercise

- Determine the ground bounce voltage for a 74HCTCMOS gate in DIP package, due to the change one output from “1” to “0”. Consider load capacitance of 20 pF.

74HCTCMOS, DIP 14 pin package: $t_{10-90} = 4.7ns$; $\Delta V_{\max} = 5V$; $L_{lead} = 8nH$

$$i(t) = C \frac{dv(t)}{dt} \quad \frac{di(t)}{dt} = C \frac{d^2v(t)}{dt^2}$$

$$|V_{GND}| = L \frac{1.52\Delta V}{T_{10-90}^2} C = 8n \times 1.52 \times 20p \frac{5}{4.7n^2} = 6,9 \frac{10^{-20}}{10^{-18}} = 69mV$$



Ground bounce

- Ground bounce can be a serious problem in high speed design. To reduce ground bounce:
 - Increase (if possible) the rise time. The 10K ECL family incorporate circuitry to do this.
 - Reduce the net inductance of return path:
 - use as short traces as possible: in TSOP and similar lead packages use the center leads; use CSP packages if possible; use the pins in the shortest row of right angle connectors
 - Use as wide conductors as possible. Virtex-4, Virtex-5, and Spartan-3 include internal ground planes or multiple ground wires spread around the chip
 - Bring the signal path as closed to return path as possible. In connectors and lead packages, return leads shall be evenly distributed among the signal leads. The worst thing to do is to put all signals at one end and all the returns at the other end.



References

- [1] Douglas Brooks, When Signal Integrity Matters,
<http://www.ultracad.com/articles/whensignalintegritymatters.pdf>
- [2] H.W. Johnson, M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993
- [3] Eric Bogatin, Signal Integrity - Simplified, Prentice Hall, 2003
- [4] Eric Bogatin, Bouncing at Ground Bounce,
http://www.bethesignal.net/bogatin/content/articles/BTS010_Bouncing_Out_Ground_Bounce.pdf
- [5] Kraig Mitzner, Complete PCB Design Using OrCad Capture and Layout, Elsevier, 2007

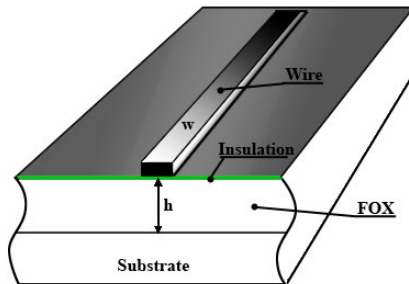


Revising last lecture

- What is ground bounce?
- What is the difference between return path and ground?
- Why packaging greatly influences ground bounce?
- Why special wire bond, tap automated bonding (TAB) and flip-chip reduces ground bounce?
- How CSP (Chip Scale Packaging) reduces ground bounce?
- How can ground bounce be reduced?

Exercise

- Consider on-chip wires where wire inductance can be calculated by:



$$h = 12000 \text{ \AA}$$

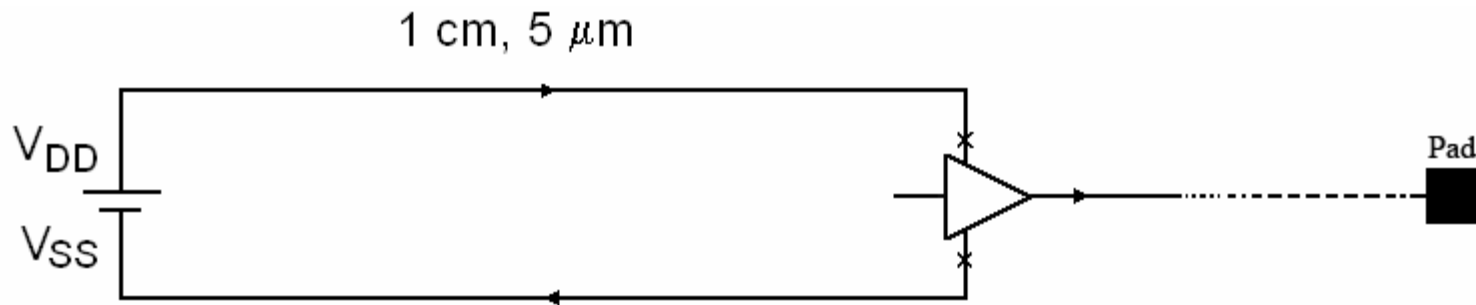
$$L = \frac{\mu}{2\pi} \ln \left(\frac{8h}{w} + \frac{w}{4h} \right)$$

μ is the magnetic permeability of the material

$$\mu = 1.257 \times 10^{-8} \text{ mH / mm}$$

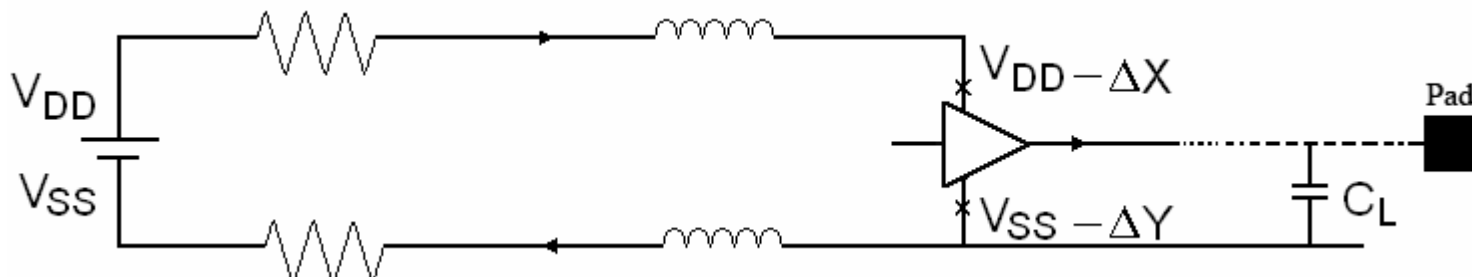
- Consider the circuit of the figure where V_{DD} and V_{SS} are connected to the gate by wires of $5 \mu\text{m}$ width and 1 cm of length, being h . Draw the equivalent circuit illustrating the parasitic inductance connecting the source gate terminals.
- Determine ground bounce and V_{DD} bounce when the output driver sources 10 mA in 1.5 ns .

Exercise



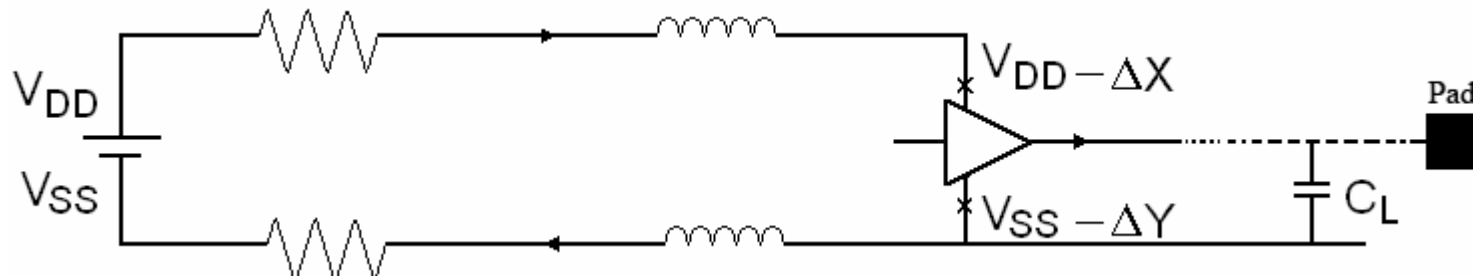
$$L = \frac{1.257 \times 10^{-8}}{2\pi} \ln \left(\frac{8 \times 12000 \times 10^{-10}}{5 \times 10^{-6}} + \frac{5 \times 10^{-6}}{4 \times 12000 \times 10^{-10}} \right) = 13.9 \text{ mH} / \text{mm}$$

$$L_{\text{total}} = 13.9 \times 10 = 139 \text{ nH}$$



Exercise

$$L_{total} = 139 \text{ nH}$$



$$\Delta X = \Delta Y = V_{drop} = 139 \times 10^{-9} \times \frac{10m}{1.5n} = 926 \text{ mV}$$

1 cm !!!